ABSTRACT

Silicon-on-insulator MESFETs have been fabricated using standard CMOS process flows and their characteristics have been measured over a temperature range of \(-180^\circ\text{C}\) to +300\(^\circ\text{C}\). From the measured data a TOM3 Spice model has been extracted. The Spice model has been used to simulate a two-stage operational transconductance amplifier and a voltage controlled oscillator. The circuit simulations show good performance over a temperature range consistent with lunar missions. In addition, MESFETs fabricated using a government SOI CMOS foundry demonstrate good radiation tolerance up to 5 Mrad(Si).

1. INTRODUCTION

Metal-semiconductor field-effect transistors, or MESFETS, have a number of advantages compared to silicon CMOS that make them attractive for extreme environment applications. These include intrinsic radiation hardness and higher breakdown voltages. MESFETs are also capable of very low power operation with excellent RF characteristics and low noise. Current MESFET technology is based on compound semiconductors and is limited to low integration levels and cannot be integrated with digital CMOS.

We have demonstrated that Si-based MESFETs can be fabricated with no changes to existing CMOS process flows. We have used a government SOI CMOS foundry [1] as well as a commercial foundry [2-4] to fabricate SOI MESFETs. The device characteristics were qualitatively identical in either case. A photograph of a MESFET used for RF measurements is shown in Fig. 1.

We present results from SOI MESFETs measured in the temperature range \(-180^\circ\text{C}\) to +300\(^\circ\text{C}\). The measured data has been used to extract a Spice model that is valid over the lunar temperature range of \(-180^\circ\text{C}\) to +130\(^\circ\text{C}\).

2. DEVICE FABRICATION

Unlike MOSFETs, which make use of a metal-oxide-semiconductor gate to form an inversion layer channel, a MESFET uses a metal-semiconductor Schottky gate that controls the current flowing in a lightly doped channel by depletion. The Schottky gate behaves as a rectifying contact and is tolerant of relatively large current flow. This fact makes the MESFET more robust than a deeply scaled MOSFET which is prone to gate breakdown if large electric fields are developed across the gate oxide. The fabrication of the Schottky gate electrode is the key step in the MESFET process and is outlined below. More details of the processing can be found in [3].

A schematic diagram showing the cross-section of the MESFET is given in Fig. 2. The MESFET Schottky gate is made of CoSi\(_2\). The CoSi\(_2\) is commonly used in CMOS processing to form the low resistance contacts to the heavily doped source and drain regions. In the case of the MESFET, the CoSi\(_2\) is also formed above a lightly doped n-well, resulting in a nearly ideal rectifying Schottky contact. The key step here is the availability of a ‘silicide-block’ step. The silicide-block is typically used to form resistive components in either silicon or poly-silicon. For the MESFETs it is used to
define the oxide spacers that separate the CoSi$_2$ that forms the Schottky gate from the CoSi$_2$ that forms the low resistance contacts to the source and drain.

The dimensions of the oxide spacers and their separation define the length of the gate, as well as the length of the channel access region from the gate to the doped source and drain regions, as shown in Fig. 2. The minimum access length was chosen to be a conservative 0.6 μm. We note that a smaller separation between the oxide spacers could probably be achieved with this 0.35 μm CMOS process, leading to shorter MESFET gate lengths.

Unlike MOSFETs, the contacts to the MESFETs are not self-aligned and the distance between the gate and the source and drain contacts (the channel access length, L$_a$) is controlled by the dimensions of the oxide spacers. A range of channel access lengths, L$_a$ = 0.6, 1, 2.2, 5 and 10 μm, were defined for different devices. The channel access length between the drain and the gate controls the breakdown voltage of the MESFET and is akin to the drift region of the LD-MOSFET [5].

3. DEVICE CHARACTERIZATION

The SOI MESFETs have been tested over a wide range of temperatures. For lunar and Martian applications, we have characterized the devices over the temperature range -180°C to +150°C. This data has been used to extract an accurate device model suitable for circuit design simulators such as Cadence. For higher temperature applications we have extended the measurements to 300°C.

3.1 SPICE Model for -180°C < T < 150°C

The drain current of the MESFET follows a good square-law dependence above threshold i.e.

$$I_{d}^{sat} \propto (V_{GS} - V_{th})^2$$  \hspace{1cm} (1)

Below threshold an exponential dependence is observed i.e.

$$I_{d}^{sat} \propto \exp(V_{GS} - V_{th} / nU_T)$$  \hspace{1cm} (2)

This device behavior is well-described by existing SPICE MESFET models such as the Curtice and TOM3 models. We have chosen to extract parameters for a TOM3 model [6] which is the most advanced MESFET model available. The model parameters are extracted from the device measurements using the IC-CAP extraction tool from Agilent [7]. More details of the model and extraction procedure can be found in [4].

Fig. 3 below shows the turn-on characteristics of the MESFET at the two extremes of temperature, i.e. -180°C and +150°C. The solid lines are the measured data while the dashed lines are the simulated results. In this above-threshold regime the difference between the measured data and the model results is never more than 5% and is generally considerably less.

![Fig. 3. The drain current as a function of gate voltage at the temperature extremes of -180°C and +150°C. The solid lines are measured data, the dashed lines are the results from the simulation. The drain voltage in each case is 2 V.](image)

The sub-threshold drain current is illustrated in Fig. 4 for a number of different temperatures. Again, very good agreement is seen between the measured and simulated results over a wide range of temperatures and currents. The only exception would be for the off-state current at the lowest temperatures, which we attribute to parasitic leakage paths. We note that the deviations are considerably less than 1 nA and therefore make little impact upon the results described here.

The MESFETs operate as depletion mode devices, and the threshold voltage, $V_{th}$, varies linearly with temperature as shown in Fig. 5. The linear temperature variation is well reproduced by the TOM3 model as shown by the solid line in Fig 5.
As a final demonstration of the MESFET SPICE model we show the measured and simulated family of curves in Fig. 6. The model has been developed to describe the small-signal and large-signal properties of a 0.6 μm gate length MESFET with \(L_g = 0.6 \mu m\) and a total width of 100 μm from 20 gate fingers. The breakdown voltage of this device exceeds 12 V. The data in Fig. 6 once again demonstrates the very reasonable agreement between measurements and modeled results over the entire range of temperature and bias voltage. Of course there is still room for optimization, as indicated by the somewhat higher current drive at room temperature and the higher output resistance at the lowest temperatures. Further optimization is possible, but the current model is sufficiently accurate to proceed with the circuit design.

Fig. 4. The drain current plotted on a log-scale as a function of gate voltage for different temperatures. The solid lines are the measured data while the symbols are the simulated results.

Fig. 5. The threshold voltage as a function of temperature. The solid line is the linear relation extracted for use in the TOM3 Spice model.

Fig. 6. The \(I_d - V_{ds}\) family of curves at -180° C, room temperature and +150° C. The gate voltages used in each case are 0.5, 0.25, 0, -0.25 and -0.5V from top to bottom. The solid lines are the measured data while the open symbols are the simulated results.
4. CIRCUIT SIMULATION

To illustrate potential applications of the SOI MESFETs we have simulated two analog circuits one being an operational transconductance amplifier (OTA) and the other a voltage controlled oscillator (VCO). The OTA is a key component in an instrumentation operational amplifier and the VCO would be used in an RF Transceiver. Both circuits have been completed to a first order design, and simulated over the temperature range -180°C < T < +130°C. Only slight variations in performance were observed. We point out here that the CMOS models are likely to be valid only over the military temperature range of -55°C to +125°C. As a consequence, although we believe that the MESFET models are accurate over the entire range, there may be discrepancies when the temperature extends beyond the limits of the available CMOS models. However, recent work has confirmed that SOI CMOS can be used for wide temperature range bias circuits using the constant inversion coefficient approach [8]

4.1 Two Stage OTA

A two stage operational transconductance amplifier (OTA) that uses MESFETs as the input differential pair in the first stage with a PMOS common-source amplifier with NMOS active load is shown in Fig. 7. The gain and phase as a function of frequency is plotted for room temperature and the two extreme temperatures of -180°C and 130°C in Fig. 8. The supply voltage was chosen to be \( V_{DD} = 3.3 \text{V} \), to be consistent with the SOI CMOS process. This circuit illustrates one of the main advantages of the SOI MESFET, namely the fact that they can be integrated with standard CMOS devices.

![Fig. 7. Schematic circuit diagram of the MESFET+CMOS operational transconductance amplifier.](image)

![Fig. 8. Gain and phase of the MESFET OTA as a function of frequency.](image)
The biasing of the OTA was chosen such that the tail current was 25 μA with a further 25 μA flowing in the common-source PMOS second stage with $I_{DC} = 5$ μA. These bias levels place the OTA in the sub-threshold (i.e. micropower) regime for all temperatures in the range -180°C to +130°C – see Fig. 4. The DC gain, unity-gain bandwidth and power consumption at RT and the temperature extremes are given in Table 1. Further optimization of the design will allow a reduction in the power consumed but without significant impact on the gain and bandwidth.

Table 1: The gain, bandwidth, current bias and power consumption of the 2-stage OTA. $V_{DD} = 3.3$V.

<table>
<thead>
<tr>
<th>Temp</th>
<th>DC Gain</th>
<th>Gain*BW Product</th>
<th>DC current</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>-180°C</td>
<td>57 dB</td>
<td>7.6 MHz</td>
<td>76.5uA</td>
<td>0.252mW</td>
</tr>
<tr>
<td>27°C</td>
<td>66 dB</td>
<td>5.4 MHz</td>
<td>55.67uA</td>
<td>0.183mW</td>
</tr>
<tr>
<td>130°C</td>
<td>52 dB</td>
<td>4.9 MHz</td>
<td>62.3uA</td>
<td>0.205mW</td>
</tr>
</tbody>
</table>

4.2 Voltage Controlled Oscillator

As a demonstrator of the RF applications of the MESFETs we have designed an LC tank-oscillator with a frequency of 1.5 GHz based on a Clapp oscillator architecture. The circuit topology is shown in Fig. 9, with the output response shown in Fig. 10. Note that with a $V_{DD}$ of 3.3 V the output voltage swing of the VCO is ~7V. This would exceed the breakdown voltage of the SOI MOSFETs, and demonstrates one of the significant advantages of the MESFET based approach. To first order, the frequency and amplitude of the Clapp oscillator are controlled by the properties of the LC tank, although the start-up condition depends upon transconductance which varies by a factor of 2 over the temperature range. There is no significant shift in the frequency or amplitude of the response. With the change in temperature, the circuit current bias changes, thereby changing the power usage. The properties of the VCO are detailed in Table 2. We note that for this preliminary design no effort was made to minimize the power consumption of the Clapp oscillator.

Table 2: The frequency, output swing, current bias and power consumption of the Clapp VCO. $V_{DD} = 3.3$V.

<table>
<thead>
<tr>
<th>Temp</th>
<th>f (GHz)</th>
<th>Output Swing (V)</th>
<th>DC current</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>-180°C</td>
<td>1.5029</td>
<td>-0.41 to 7.02</td>
<td>671.75uA</td>
<td>2.22mW</td>
</tr>
<tr>
<td>27°C</td>
<td>1.5032</td>
<td>-0.4 to 7.01</td>
<td>671.801uA</td>
<td>2.22mW</td>
</tr>
<tr>
<td>130°C</td>
<td>1.5035</td>
<td>-0.185 to 6.8</td>
<td>773.142uA</td>
<td>2.55mW</td>
</tr>
</tbody>
</table>

Fig. 9. The Clapp circuit topology used for the VCO design

Fig. 10. Envelope function of the VCO output response. $T=27^\circ$C.
5. CHARACTERIZATION UP TO 300°C

To better understand the temperature limits of the SOI MESFETs we have extended the high temperature measurements to 300°C. The gate and drain currents as a function of gate voltage are shown in Fig. 11. At room temperature the ratio of on-state to off-state drain current is ~4000. This ratio falls to ~3 at 300°C. The increase in off-state drain current with increasing temperature can be attributed to the increase in the reverse bias gate leakage current. It is apparent from the data in Fig. 11 that the Schottky gate becomes more conducting at elevated temperatures and the non-linear (i.e. rectifying) nature of the gate is diminished. We attribute much of the gate leakage current to edge effects and with further optimization it might be possible to further decrease the off-state drain current. However, from these measurements we speculate that the highest operating temperature for MESFET-based circuits will be 250°C where the off-state ratio is > 10. We note here that the MESFETs appear to suffer no permanent damage after several hours of heating to 300°C. The drain and gate currents were re-measured at room temperature after thermal cycling and only minimal changes were observed.

![Graph](image)

Fig. 11. The drain currents (solid lines) and gate currents (dashed lines) as a function of gate voltage measured at elevated temperatures. V_{ds} = 2V.

6. RADIATION TESTING

The radiation response of SOI MESFETs fabricated using the government CMOS process have been tested by exposure to 50 keV x-rays up to a total ionizing dose of 5 Mrad(Si). These results are summarized below. More detail can be found in [1].

The turn-on characteristics of the MESFETs are shown in Fig. 12. Prior to irradiation the threshold voltage of the device was approximately ~0.5V. To better understand the operation of the device, we have developed a numerical model for the SOI MESFET - see [1]. The values of device parameters that are accurately known, such as gate length, SOI thickness, channel doping etc., are used for the simulation. The parameters that are not known prior to simulation are the fixed oxide charge density, N_{ox}, and the interface trap density, N_{it}, both of which are associated with the non-ideal interfaces between the SOI channel and the BOX layer below and the spacer oxides above. These parameters are used as fitting parameters in the model. To reproduce the pre-radiation data shown in Fig. 12 we have used a fixed charge density, N_{ox} of 0.4x10^{11} cm^{-2}, and an interface state density N_{it} of 6x10^{11} cm^{-2}. A single trap level at an energy 0.48 eV below the conduction band edge was used, although the precise location of the trap level did not change the simulation significantly. Although this assignment of interface trap states is empirical it adequately reproduces the slope of the I_d vs V_g curve.

Radiation tests were performed on unpackaged die using an Aracor 4100 Semiconductor Irradiation System. The Aracor system emits x-rays at energies from 10 to 60 keV and these x-rays are then directed out of an aperture towards the chuck and the sample. For these experiments, the electron energies were 50keV. During irradiation, the devices were contacted using a probe card and electrical measurements were made immediately after irradiation. Arbitrary bias could be applied during the irradiation but for the results described here all contacts were grounded during the x-ray exposure. The total dose test plan selected follows the military standard 883E, method 1019.6. The dose rate is set to 20 krad(Si)/min up to 400 krad(Si) total dose. Beyond 400 krad(Si) the dose rate is increased to 40 krad(Si)/min.

The SOI MESFET has a buried oxide that will be susceptible to radiation induced trapped charge. The spacer oxide on the top surface of the MESFET (see Fig. 2) will also be susceptible to radiation. To model the effect any such trapped charge will have on the
threshold voltage of the MESFET, we assume that it can be treated as fixed charge, \( N_{\text{ox}} \), because previous work on SOI BOX charge trapping indicates that generated carriers do not travel far from their generation site [9], [10]. The data in Fig. 12 shows the turn-on characteristics (\( I_d \) vs. \( V_{gs} \)) of the MESFET after the device has received a total ionizing dose of 5 Mrad(Si). After irradiation the threshold voltage has shifted to approximately \(-1\) V.

![Graph of Drain Current (mA) vs. Gate Voltage (V)](image)

Fig. 12. The drain current as a function of gate voltage for a MESFET of gate length 0.6 \( \mu \)m. Prior to irradiation the threshold voltage is approximately \(-0.5\) V. After a TID of 5 Mrad(Si) it shifts to \(-1\) V. The circles and squares show the simulated results before and after irradiation, respectively. \( V_{th} = 0.5 \) V.

The observed shift in threshold voltage is consistent with an increase in the fixed oxide trapped charge density in the buried oxide and, presumably, in the surface spacer oxide. The fixed oxide charges will be positive, and extra free electron charge will be attracted into the channel from the n’ source/drain contacts to ensure charge neutrality. A larger reverse bias will have to be applied to the gate to deplete the increased free electron concentration in the channel, resulting in a more negative threshold voltage. The shift in threshold, \( \Delta V_{th} \), due to an increase in trapped oxide charge, \( \Delta N_{\text{ox}} \), can therefore be written as

\[
\Delta V_{th} = - e \frac{\Delta N_{\text{ox}}}{C_{\text{gate}}}
\]

where \( C_{\text{gate}} \) is the gate capacitance per unit area. We have taken the model used to describe the pre-irradiation data and modified it to fit the data after a TID of 5 Mrad(Si). The data in Fig. 12 suggests a simple translational shift in the \( I_d \) vs \( V_{gs} \) curve as a result of a change in threshold voltage. There is no obvious shift in the slope of the \( I_d \) vs \( V_{gs} \) curves and for this reason we believe that any increase to the interface trap density after irradiation is negligible. Indeed, the fit to the data after irradiation shown by the open squares in Fig. 12 was obtained simply by increasing \( N_{\text{ox}} \) from \( 0.4 \times 10^{11} \) cm\(^2\) to \( 3.4 \times 10^{11} \) cm\(^2\).

The shift in threshold voltage, \( \Delta V_{th} \), is plotted as a function of TID in Fig. 13. The data in Fig. 13 suggests that the threshold voltage shift is initially linear with increasing TID but eventually saturates for a high enough TID. This saturation in the threshold shift has been observed in SOI MOSFETs [11], [12] and is attributed to a saturation in the fixed oxide charge density at high radiation doses.

![Graph of \( \Delta V_{th} \) vs. Total Ionizing Dose (Mrad)](image)

Fig. 13. The shift in the threshold voltage of the Schottky top gate as a function of total ionizing dose.

7. CONCLUSIONS

We have demonstrated that CMOS compatible MESFETs can be fabricated alongside conventional CMOS. The MESFETs show excellent device performance over the wide temperature range -180°C to +150°C. We have extracted an accurate Spice model and applied it to the design of a two-stage OTA and a 1.5 GHz VCO. The MESFETs operate up to 300°C although high off-state current limits the useful application of the current generation of devices to 250°C. With further optimization it may be possible to
extend the operating temperature. The MESFETs show good radiation tolerance with a – 0.5 V shift in threshold voltage after exposure to a TID of 5 Mrad(Si). The high voltage capability, combined with the wide temperature operating range and radiation tolerance suggest that CMOS compatible SOI MESFETs will be suitable for applications that require high-performance extreme environment electronics.

8. REFERENCES


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