ANALOG/DIGITAL CIRCUIT DESIGN IN SiGe FOR SPACE APPLICATIONS

Tiejun Cao, Electrical Engineering Dept., University of Arkansas, tcao@uark.edu
Richard Broughton, Electrical Engineering Dept., University of Arkansas, rbrough@uark.edu
Jayamadhuri Penumarthi, Computer Science and Computer Engineering Dept., University of Arkansas, jpenuma@uark.edu
Jia Di, Computer Science and Computer Engineering Dept., University of Arkansas, jdi@uark.edu
H. Alan Mantooth, Electrical Engineering, University of Arkansas, mantooth@uark.edu
Contact Author: Jia Di; ENGR 311, CSCE Dept., University of Arkansas; Fayetteville, AR 72701

***Abstract* – This paper reports on both analog and digital circuit designs in Silicon-Germanium (SiGe) that are designed to operate over the lunar temperature extremes. The design of a variable gain amplifier (VGA), and digital circuits using synchronous and asynchronous logic styles for comparison working under low temperatures are described.**

I. Introduction

Silicon-Germanium (SiGe) BiCMOS technology has demonstrated the capability to provide excellent high-performance characteristics with very low noise, high power gain, and excellent linearity. The bandgap engineering employed in the design of SiGe HBTs generally favors their operation at cryogenic temperatures. Thus, SiGe circuits hold much promise for applications to the extreme environments of space applications. Analog and digital circuits are designed in SiGe to operate over the lunar temperature extremes.

Sensor systems are critical parts for space exploration vehicles. In particular, to improve the accuracy of collected data, the signals output from sensors should be pre-processed prior to transmission and further processing. The high variability of the sensor's signal output has to be regulated so that a suitable signal level can be applied to subsequent circuitry such as analog-digital converters (ADCs). For that reason, the VGA plays a fundamental role in optimizing system capacity. Sensors are often exposed directly to the environment in order to perform their function. The environment of space can exhibit large temperature swings.

VGAs are widely used in wireless communications, industrial scanning, radar, ultrasound, and speech-analysis applications that require a wide dynamic range of a continuous voltage. There are many different topologies used to realize VGAs. Common approaches use analog multipliers [1]-[3], variable transconductance [4], [5], variable loads [4], [6], variable feedback [7], [8], and attenuator networks [9]. In this paper, a VGA for wide temperature applications is proposed. It is based on a variable gain transconductance topology. The gain of the VGA is designed to vary from 1 to 50 per requirements of the overall system.

While working under low temperatures, CMOS digital circuits are able to operate faster because of better carrier mobility in the device's channel. Since sometimes this performance enhancement is either not required or even unwanted, it provides the opportunity to reduce power consumption. The circuit will achieve the same performance under lower supply voltage while operating at low temperatures. Since power consumption of CMOS digital circuits is roughly proportional to V_{DD}^2, the use of lower supply voltage will produce much lower power consumption, which is a critical consideration for space applications. Asynchronous circuits have the potential for even better power efficiency than normal synchronous circuits. Synchronous circuits have to toggle clock lines and charge signals in those circuit blocks that are not processing useful data for a computation. For asynchronous circuits, even though they typically need more transistors to achieve equivalent functionality, only the transistors in the area of a current computation will be actively drawing power. Asynchronous circuits are also more adaptable to changes in temperature and supply voltages. A synchronous circuit would have to adjust its clock to the worse case critical path delay for the entire temperature and voltage range in which the circuit is to operate. Since asynchronous circuits use handshaking signals to sense completion, they automatically adjust to the delay changes caused by these variations.

Three simple pipelined circuits have been designed in synchronous logic and two asynchronous logic styles, namely, delay-insensitive and bounded-delay. The bounded-delay circuit used the traditional micropipeline structure approach [10]. In this methodology, standard Boolean-based combinational logic is combined with asynchronous control which employs C-elements. The delay-insensitive circuit design used NULL Convention Logic ™ (NCL) [11]. This type of asynchronous design employs dual-rail encoding to represent data and NULL states in order to incorporate control information to data as well as to provide hysteresis.

II. VGA Circuit Description

The block diagram of the VGA is shown in Fig. 1. The VGA consists of a VGA core A1 and a buffer circuit A2. A1 is based on a classic differential pair, whose transconductance is adjusted by varying the tail bias current I_{CTRL}, as shown in Fig. 2 [12]. A2 can provide a single-ended output and cancel a common-mode voltage variation at the output of A1. In order to make the gain independent of temperature, "ratioing" of the resistors and currents is implemented. The gain of the VGA is

$$A = \frac{R_2}{R_1}\frac{I_{CTRL}}{I_1}\frac{R_L}{R_E} \quad (1)$$

A. VGA Core

The circuit of VGA core A1 has two stages. The first stage has a constant gain. The feedback within the first stage linearizes the overall circuit gain. The second stage is a traditional differential pair. The transconductance of the two transistors in this pair is controlled by I_{CTRL}, which is the current to control the gain of the VGA core.

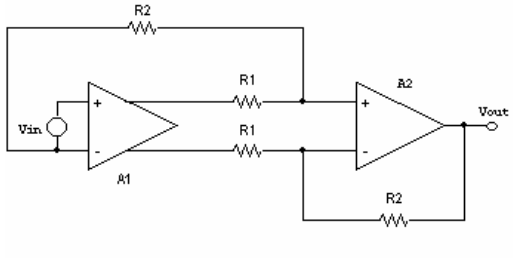

Fig. 1. The block diagram of the VGA circuit.

The gain of the second stage is

$$A_{V2} = -g_m R_L \quad (2)$$

where

$$g_m = \frac{I_{ctrl}}{2V_T}$$

thus,

$$A_{V2} = -\frac{I_{CTRL}}{2V_T}R_L \quad (3)$$

For the first stage, Q3, Q4, Q5 and Q6 act as a feedback circuit for the differential pair Q1and Q2. Transistor pairs Q3, Q5 and Q4, Q6 form CC-CE configurations with $g_m = \frac{I_1}{V_T}$.

Therefore, the feedback factor is given as follows,

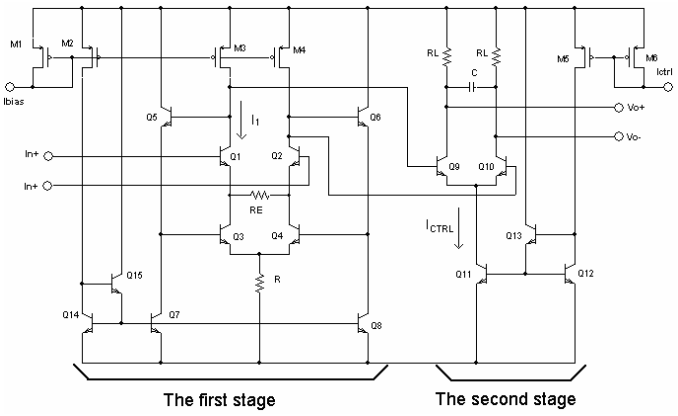

Fig. 2. The schematic of VGA core circuit.

$$\beta = g_m \frac{R_E}{2} = \frac{I_1}{V_T}\frac{R_E}{2}. \quad (4)$$

The open loop gain of the Q1-Q2 differential pair is assumed large, thus

$$A_{V1} \cong \frac{1}{\beta} = \frac{2V_T}{I_1.R_E}. \quad (5)$$

As a result, the overall gain is [10]

$$A_1 = A_{V1}A_{V2} = \frac{2V_T}{I_1.R_E}\frac{I_{CTRL}}{2V_T}.R_L = \frac{I_{CTRL}}{I_1}\frac{R_L}{R}. \quad (6)$$

To achieve a constant gain over a wide temperature range, the ratio $\frac{I_{CTRL}}{I_1}$ and $\frac{R_L}{R_E}$ must be held constant.

Reducing the mismatch between R_L and R_E is critical to maintaining a constant ratio. R_L and R_E are chosen as 4.4 kΩ and 1 kΩ, respectively. An off-chip current reference source was used to produce I_{CTRL} and I_1 for testing purposes, but an on-chip current reference is the subject of additional wide temperature design activity.

B. Buffer Circuit

The variable control current leads to a common-mode voltage variation at the output of the VGA core. A buffer (A2 from Fig. 2) shown in Fig. 3 is introduced in order to cancel this effect and provide a single-ended output.

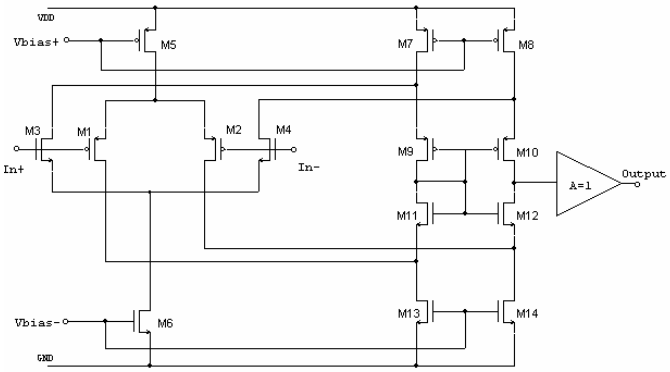

Fig. 3. The schematic of the buffer circuit (A2 in Fig. 1).

The folded cascode amplifier provides a wide-band frequency response and high gain with a single stage. However, its high output resistance makes it difficult to interface with other circuits. A unity gain buffer at the output of the folded cascode circuit addresses this issue.

The low frequency gain of the folded cascode stage is

$$A_V = G_m R_0 \quad (7)$$

where G_m is the total transconductance of the input stage, which is given by [13]

$$G_m = g_{m1} + g_{m3}. \quad (8)$$

The R_0 is the small-signal resistance looking into the drain of M10 and M12, thus (7) becomes

$$A_V = (g_{m1} + g_{m3})(g_{m10}r_{08}r_{010} \,//\, g_{m12}r_{014}r_{012}). \quad (9)$$

In order to achieve an open-loop gain over temperature that remains sufficiently large such that the closed-loop gain of A2 remains determined by the feedback factor (i.e., the ratio of two resistor values here), the authors chose to maintain a constant inversion coefficient (IC) (defined below). A constant inversion coefficient has the advantage of canceling out

temperature variation due to changing thermal voltage. For each transistor, the moderate inversion characteristic current I_S is given by,

$$I_S = \frac{2\mu C_{ox} V_T^2}{k}(\frac{W}{L}) \quad (10)$$

The *IC* for each transistor may be calculated as the ratio of drain current to the moderate inversion characteristic current as follows [14],

$$IC = \frac{I_D}{I_S} \quad (11)$$

A transistor having *IC* > 10 clearly operates in strong inversion region and has a transconductance proportional to the square root of drain current. A transistor having *IC* < 0.1 clearly operates in weak inversion region and has a transconductance proportional to the drain current. Generally, *IC* = 1 is the crossover point between weak and strong inversion.

In weak inversion, the transconductance of the transistors is

$$g_m = \frac{kI_D}{V_T} \quad (12)$$

where *k* is the subthreshold gate coupling coefficient. A typical value of *k* is 0.7. In strong inversion region, g_m is

$$g_m = \sqrt{2\mu C_{ox}(\frac{W}{L})I_D} \quad (13)$$

Therefore, the relative transconductance can be derived as follows,

$$\frac{g_m}{I_D} = \frac{kI_D/V_T}{I_D} = \frac{k}{V_T} \quad (14)$$

in weak inversion, and

$$\frac{g_m}{I_D} = \frac{\sqrt{2\mu C_{ox}(\frac{W}{L})I_D}}{I_D} = \sqrt{\frac{2\mu C_{ox}(\frac{W}{L})}{I_D}} \quad (15)$$

in strong inversion.

We can rewrite (9) in terms of the relative transconductance and drain current as follows,

$$A_V = (g_{m1}+g_{m3})\left[g_{m10}\frac{V_A}{I_{D8}}\frac{V_A}{I_{D10}} // g_{m12}\frac{V_A}{I_{D14}}\frac{V_A}{I_{D12}}\right] \quad (16)$$

Note that we have $g_{m10} = g_{m12}$, $I_{D8} = I_{D14}$, and $I_{D10} = I_{D12}$, Therefore, the gain of the buffer becomes

$$A_V = \frac{1}{2}\frac{g_{m10}}{I_{D10}}(\frac{g_{m1}}{I_{D8}}+\frac{g_{m3}}{I_{D8}}).V_A^2 \quad (17)$$

In strong inversion, the gain is

$$A_V = \sqrt{\frac{\mu_p C_{ox}(\frac{W}{L})_{10}}{2I_{D10}}}\left[\frac{\sqrt{2\mu_p C_{ox}(\frac{W}{L})_1 . I_{D1}}}{I_{D8}}+\frac{\sqrt{2\mu_n C_{ox}(\frac{W}{L})_3 I_{D3}}}{I_{D8}}\right]V_A^2. \quad (18)$$

In weak inversion, the gain is

$$A_V = \frac{1}{2}\left(\frac{kV_A}{V_T}\right)^2\left[\frac{I_{D1}}{I_{D8}}+\frac{I_{D3}}{I_{D8}}\right]. \quad (19)$$

From (10), we have

$$\mu C_{ox}(\frac{W}{L}) = \frac{kI_S}{2V_T^2}. \quad (20)$$

Therefore, (18) becomes

$$A_V = \frac{1}{2}(\frac{KV_A}{V_T})^2\sqrt{\frac{1}{k}\frac{1}{IC_{10}}}\left[\sqrt{\frac{1}{k}\frac{1}{\eta_1}\frac{1}{IC_1}}+\sqrt{\frac{1}{k}\frac{1}{\eta_3}\frac{1}{IC_3}}\right] \quad (21)$$

where $\eta_1 = (\frac{I_{D8}}{I_{D1}})^2$ and $\eta_3 = (\frac{I_{D8}}{I_{D3}})^2$.

From (19), in weak inversion, we also have

$$A_V = \frac{1}{2}(\frac{kV_A}{V_T})^2\left[\sqrt{\frac{1}{\eta_1}}+\sqrt{\frac{1}{\eta_3}}\right] \quad (22)$$

Since the transistors are identical, η_1 and η_3 are constant over temperatures.

From (21) and (22), the open loop gain of the buffer over temperature is primarily affected by V_T if *IC* is kept constant. The overall gain of the buffer circuit depends on the ratio of the feedback resistors and thus the gain is constant over temperature.

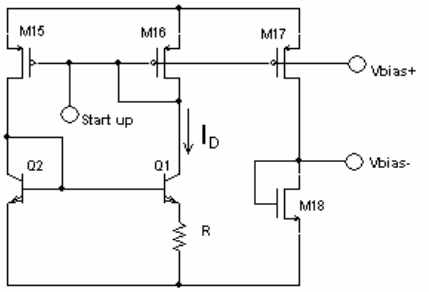

Fig. 4. The bias configuration for the buffer circuit.

To keep $IC = \frac{I_D}{I_S}$ constant, a proportional to absolute temperature (PTAT) current source bias is used. Because I_S depends on V_T^2 which is strongly dependent on temperature, I_S will increase when temperature increases. Therefore, the bias current I_D also has to increase with the temperature. From Fig. 4, we have

$$I_{C2} = \frac{V_T}{R}\ln(N) \quad (23)$$

where *N* is the ratio of base-emitter junction areas of Q1 and Q2.

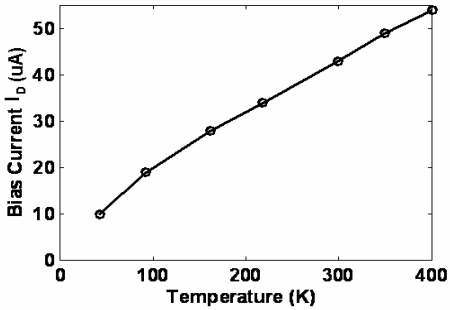

Fig. 5. The bias current of buffer circuit versus temperature.

Fig. 5 shows the relationship between the bias current and temperature. *N* equal to 5 is chosen from the simulation results in order to keep *IC* constant.

III. Experimental Results

The VGA circuit was fabricated in the IBM SiGe 5AM BiCMOS process. A die photograph of the VGA circuit is shown in Fig. 6. The circuit performed over a wide temperature range from 43 K to 300 K. There are four main specifications: gain (1-50), bandwidth (> 1MHz), slew rate (10 V/µs) and input capacitance (< 25pF). These measured results met the main design specifications. Fig. 7 shows the VGA gain characteristics at different temperatures. Fig. 8 describes the VGA slew rate characteristics over the wide temperature range.

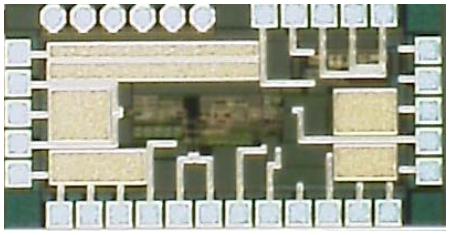

Fig. 6. Die photograph of the VGA.

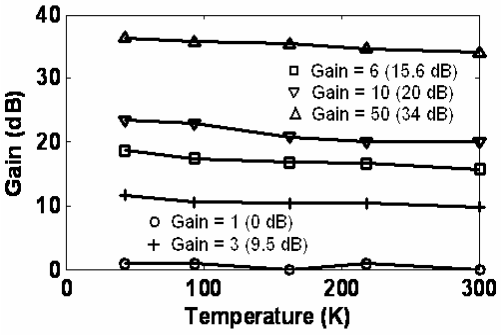

Fig. 7. VGA gain characteristics over cryo temperatures.

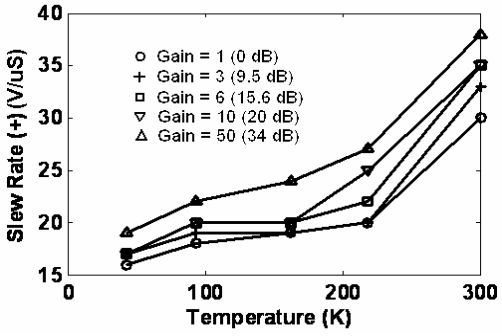

Fig. 8. VGA slew rate characteristics over cryo temperatures.

IV. Digital Circuit Description

A. Pipelined Circuit Comparison

A supply voltage scalability comparison of regular synchronous digital logic and the two asynchronous digital logic styles is being performed in order to determine which logic style would be best suited to extreme environment space application. So far simulations of simple pipelined circuit structures suggest that there is an advantage to using asynchronous logic.

Simple Pipelines Circuits

In order to make the comparison as fair as possible, the same circuit topology was constructed with all three design methods. The topology chosen was a small pipeline structure that is shown in Fig. 9 which contains three register stages with full adders between them. Thus the circuits performed the same function on the data, but each circuit was constructed based on its different design methodology.

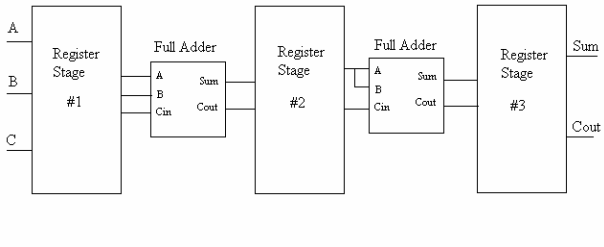

Fig. 9. Topology for comparison circuits.

Simulation Results

The lowest operating voltage levels for all three circuits at the three cold temperature points as well as room temperature are shown in Table 1. In these simulations the two asynchronous circuits were both able to operate at 0.2 volts lower supply voltage then the synchronous circuit at the colder temperatures. The NCL circuit performed particularly well in these simulations, and was able to operate at even lower supply voltages then the bounded delay circuit.

Table 1. Simulated lowest operating voltages

	25 °C	-111 °C	-180 °C	-230 °C
Synchronous Circuit	1.35 V	1.35 V	1.28 V	1.31 V
NCL Circuit	1.05 V	1 V	0.95 V	1 V
Bounded Delay Circuit	1.5 V	1.1 V	1.1 V	1.08 V

These circuits have been fabricated and experimental measurements will be taken to validate the results of the simulation. While this is happening, the comparison has been taken a step further by designing an asynchronous microcontroller to be compared to a synchronous counterpart.

B. Design of Asynchronous Microcontroller

A dual-Rail 8-bit asynchronous microcontroller has been designed using the delay- Insensitive NULL Convention Logic ™ (NCL) paradigm. The microcontroller mainly consists of Instruction Decoder, Arithmetic Logic Unit (ALU), and Register File. It has no memory and the opcode is the primary input. There are two interfacing circuits (wrappers) at the input and output to communicate with any synchronous devices.

Instruction Set:

Operation Type	*Instruction Type*	*Mnemonics*	*Description*
Data Transfer	LOAD	LD Rx	Store data into Rx register.
	MOVE	MOV Rx, Ry	The contents of Ry is copied to Rx
	OUT	OUT Rx	The contents of Rx are output from microcontroller
Logical	AND	AND Rx ,Ry	The operands of Rx and Ry are ANDed and result is stored in Rx.
	OR	OR Rx ,Ry	The operands of Rx and Ry are ORed and result is stored in Rx
	XOR	XOR Rx ,Ry	The operands of Rx and Ry are XORed and result is stored in Rx
Arithmetic	ADD	ADD Rx ,Ry	The operands of Rx and Ry are ADDed and result is stored in Rx
	NOT	NOT Rx	The operands of Rx are complemented.

The block diagram of the microcontroller is shown in Fig. 10.

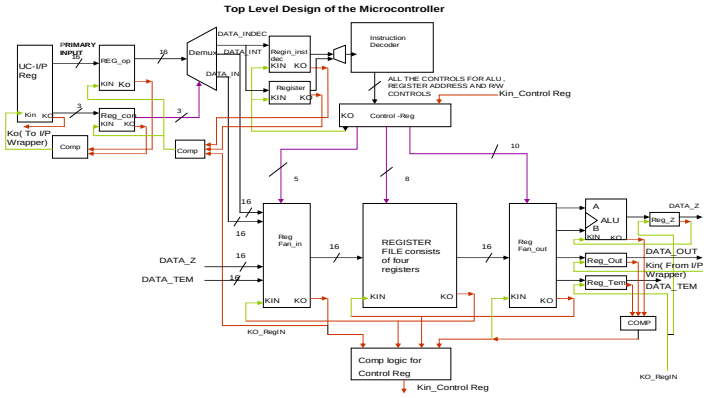

Fig. 10. The block diagram of the microcontroller.

Instruction Decoder

It's a combinational circuit consists of threshold gates. The instructions are the inputs and the outputs are the controls for the ALU and Register file.

ALU

The ALU consists of an adder, a logic unit and a NOT block. It's a pipelined structure. The adder is a 2NCL 8-bit Ripple Carry Adder which performs addition on the 8-bit dual-rail input. The Logic unit performs AND, OR and XOR operations.

Register File

The Register file consists of four general-purpose Registers and one temporary register. The general-purpose registers have consume/produce Structure, which consists of phase inverted storage /consume registration stage followed by a produce registration stage, both coordinated by a two value control. The temporary register supports the MOVE operation and is a simple ring structure.

At this time the cold temperature simulations of this asynchronous microcontroller as well as its synchronous counterpart are still being performed. The preliminary results show the asynchronous microcontroller is able to work at lower supply voltage under low temperature.

V. Conclusion

This paper demonstrated the operating principle and experimental results of a VGA circuit featuring temperature stable operation, as well as the advantage of asynchronous logic over synchronous counterpart on supply voltage scaling under low temperature for designing digital electronics for space applications. The circuit works over a wide range of temperatures. Maintaining a constant inversion coefficient provided a reasonable tradeoff to maintain gain versus temperature. Measurement results satisfy the main specifications. Future work includes circuit optimization and reducing noise.

References

[1] T. Pan, and A. A. Abidi, "A 50-dB Variable Gain Amplifier using Parasitic Bipolar Transistors in CMOS," *IEEE Journal of Solid-State Circuits*, vol.24, no.4, pp. 951-961, August 1989.

[2] M. Franciotta, G. Colli, and R. Castello, "A 100-MHz 4-mW Four-Quadrant BiCMOS Analog Multiplier," *IEEE Journal of Solid-State Circuits*, vol.32, no.10, pp.1568-1572, Oct. 1997.

[3] J. Hakkinen, T. Rahkonen, and J. Kostamovaara, "A 100-MHz to 1 GHz Variable Gain Amplifier in a 8 GHz 1.2mm BiCMOS Process," *Analog Integrated Circuits and Signal Processing*, vol.15, no.2, pp.169-181, Feb. 1998.

[4] R. Gomez, and A. A. Abidi, "A 50-MHz CMOS Variable Gain Amplifier for Magnetic Data Storage Systems," *IEEE Journal of Solid-State Circuits*, vol.27, no.6, pp.935-939, June 1992.

[5] J. J. Rijns, "CMOS Low-Distortion High Frequency Variable Gain Amplifier," *IEEE Journal of Solid-State Circuits*, vol.31, no.7, pp.1029-1034, July 1996.

[6] T.H. Hu, and P. R. Gray, "A Monolithic 480 Mb/s Parallel AGC/Decision/Clock Recovery Circuit in 1.2-mm CMOS," *IEEE Journal of Solid-State Circuits*, vol.28, no.12, pp.1314-1320, Dec 1999.

[7] J.N. Babanezhad, and R. Gregorian, "A Programmable Gain/Loss Circuit," *IEEE Journal of Solid-State Circuits*, vol.22, no.6, pp.1082-1090, Dec 1987.

[8] A.L. Wittenberg, M.L. Simpson and G. R. Young, "A CMOS Variable Gain Amplifier for PHENIX Electromagnetic Calorimeter and RICH Energy Measurements," *IEEE Trans. Nuclear Sci*, vol.44, no.3, pp.326-330, June 1997.

[9] J. Bales, “An BiCMOS Digitally-Controlled Variable Gain Wideband Amplifier,” *Proceedings of the IEEE BiCMOS Circuits and Technology Meeting, pp. 84-87, 1997*.
[10] Ivan E. Sutherland, “Micropipelines” *Communications of the ACM*, vol. 32, no. 6, pp. 720-738, June 1989.
[11] K. Fant, *Logically Determined Design: Clockless System Design with NULL Convention Logic™*, 1st ed., New York: Wiley-Interscience, pp. 36-41, 2005.
[12] F. Carrara, P. Filoramo, and G. Palmisano, “High-dynamic-range decibel-linear IF variable-gain amplifier with temperature compensation for WCDMA applications,” *Circuits and Systems, 2003. ISCAS '03.*, vol.1,SC-9, pp. I289-I292, May 2003.
[13] Adel S. Sedra, Kenneth C. Smith, *Microelectronic Circuits*, Oxford University Press, New York, 2004.
[14] D. M. Binkley, C. E. Hopper, S. D. Tucker, B. C. Moss, J. M. Rochelle, and D. P. Foty, “A CAD Methodology for Optimizing Transistor Current and Sizing in Analog CMOS Design,” *IEEE Trans. Computer-Dided Design of Integrated Circuits and Systems*, vol.22, no.2, pp.225-237, Feb. 2003.