# Electronics Packaging for Extreme Environments

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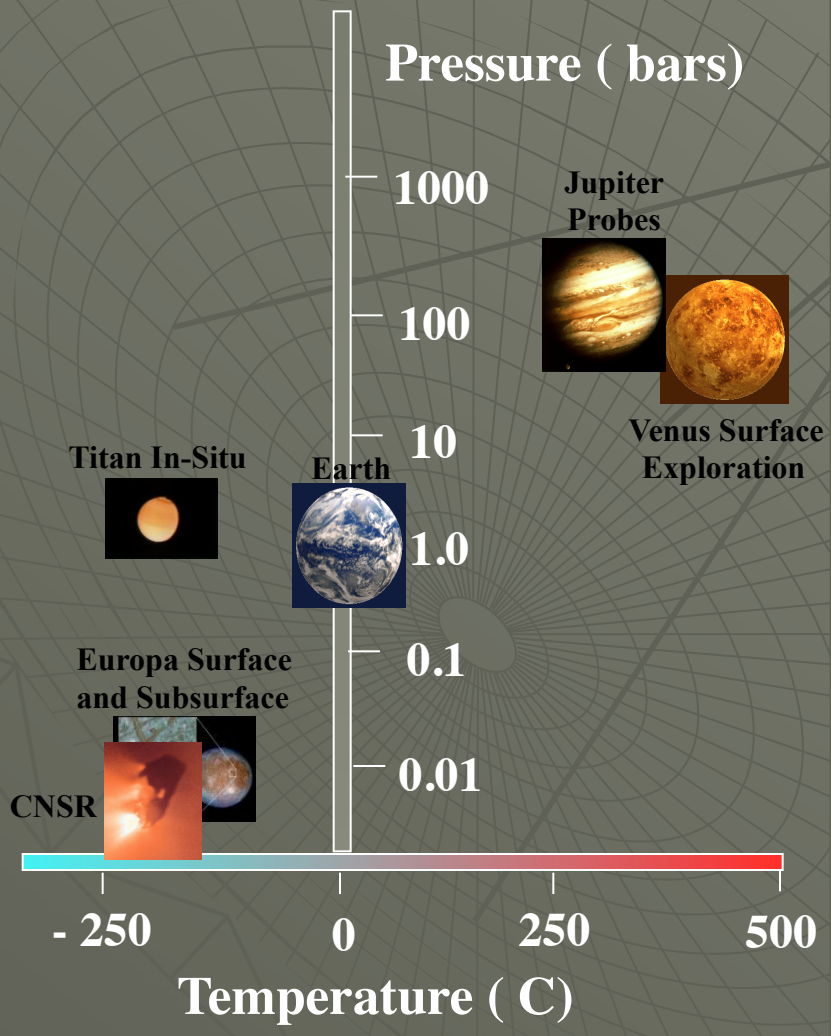
# Outline

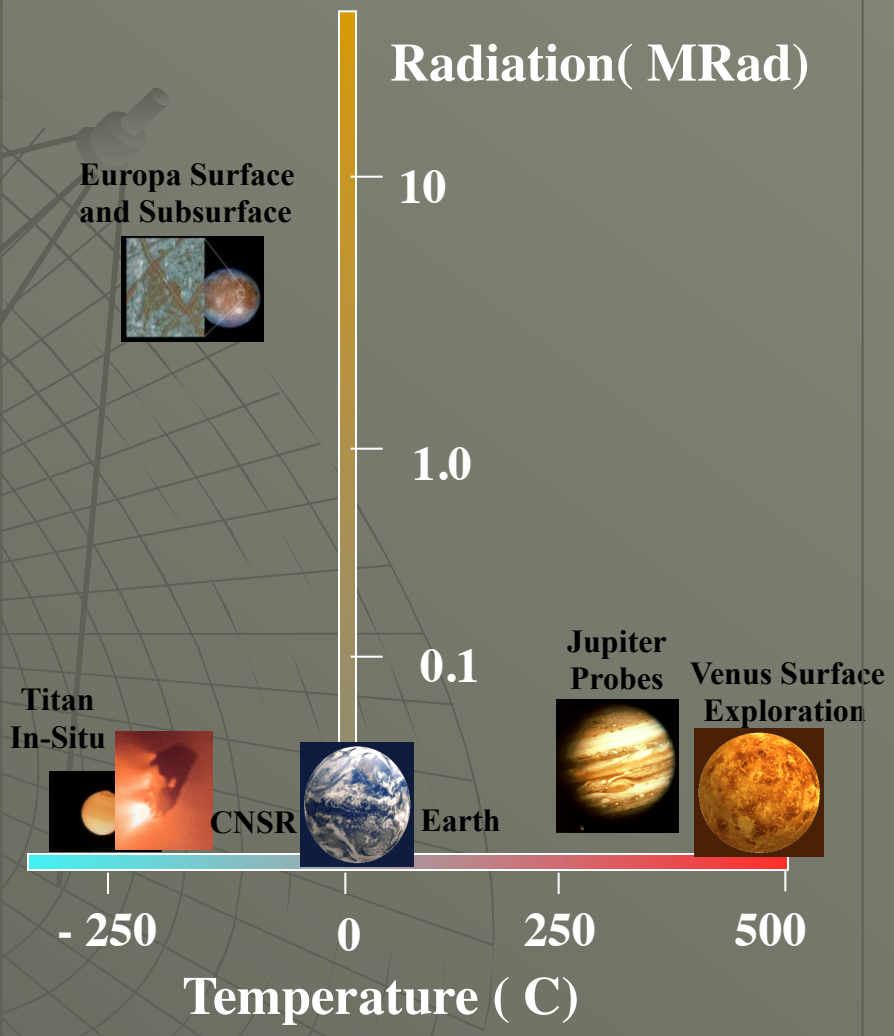
- Introduction
- Devices
  - Passive
  - Active
- Packaging
  - Low Temperature
  - High Temperature
- Summary

# Exploration: Space

## Pressure vs. Temperature




## Radiation vs. Temperature




Courtesy: Mohammad M. Mojarradi, JPL

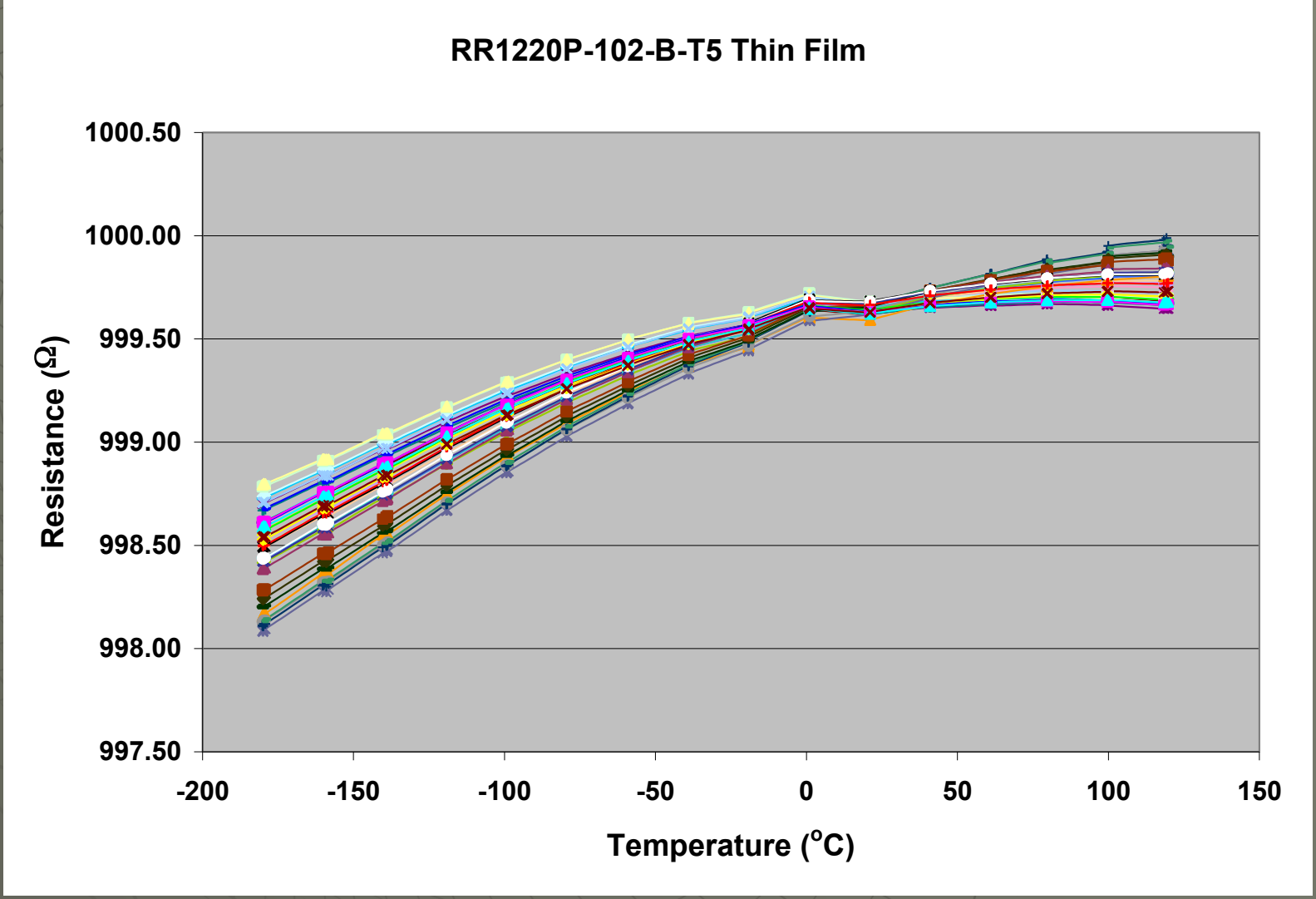
# Current Designs

- Low Temperature
  - Warm electronics boxes
  - Centralized design
  - Lots of wiring
  - Power consumption
  - Some things have to be outside the Box
- High Temperature
  - Dewars
  - Phase change materials
  - Limited operating life
  - Lens a source of heat ingress
  - Some things have to be outside the Dewar

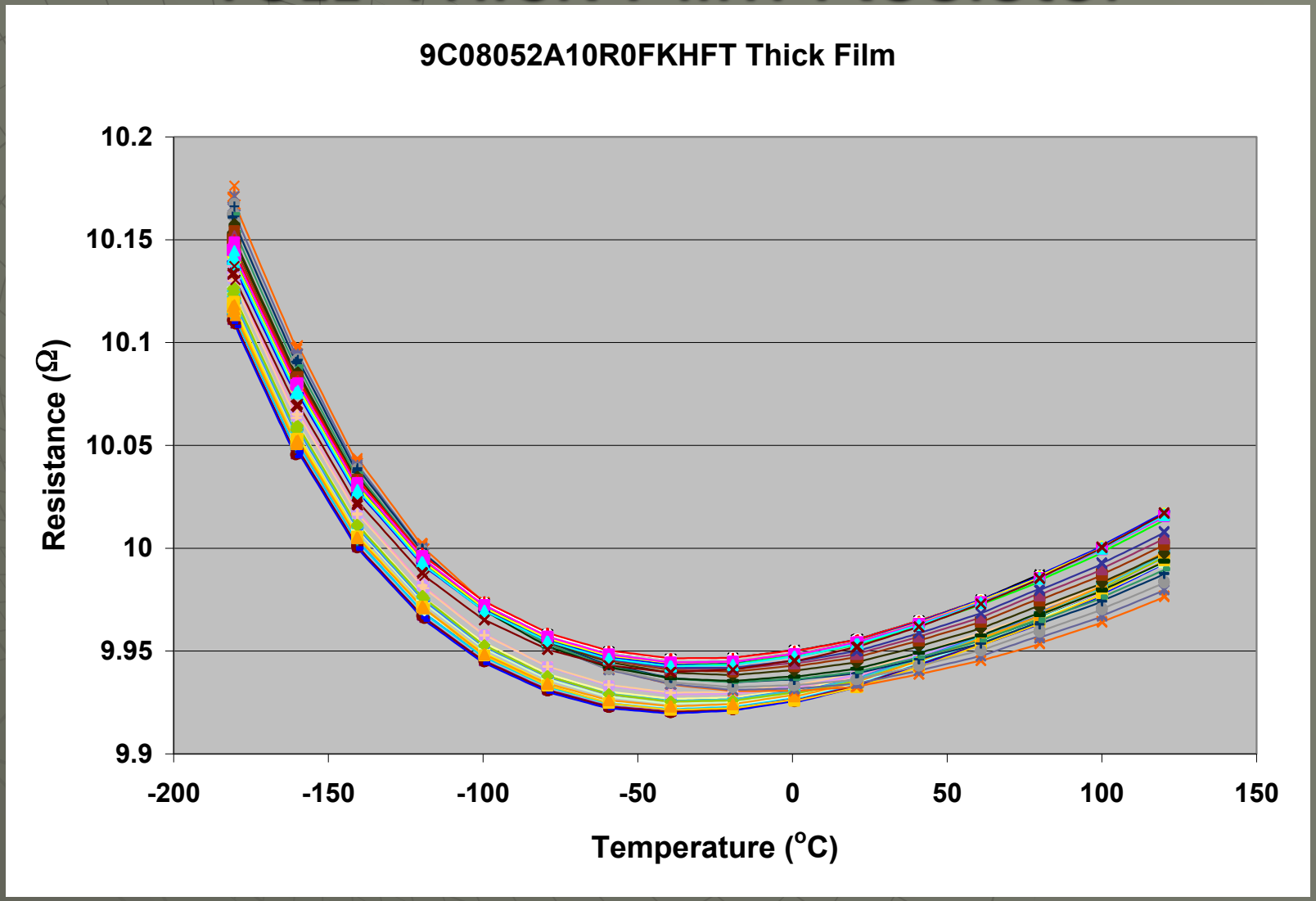
# With Extreme Environment Electronics

- Distributed architectures
  - Less wiring
- Longer mission life at high temperatures
- Less power consumption

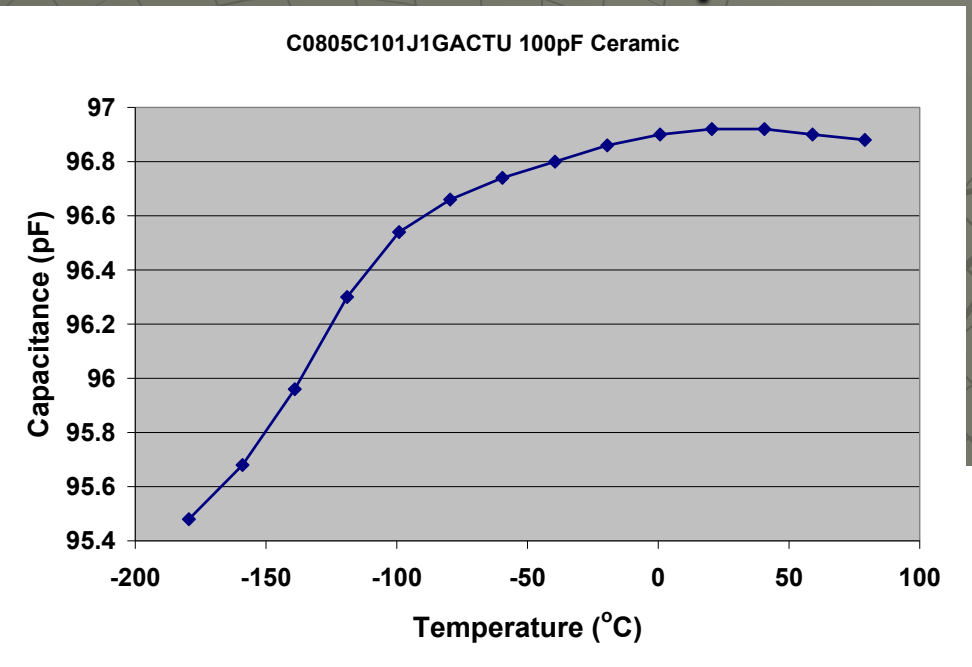
# Passive Components: 1kΩ Thin Film Resistor

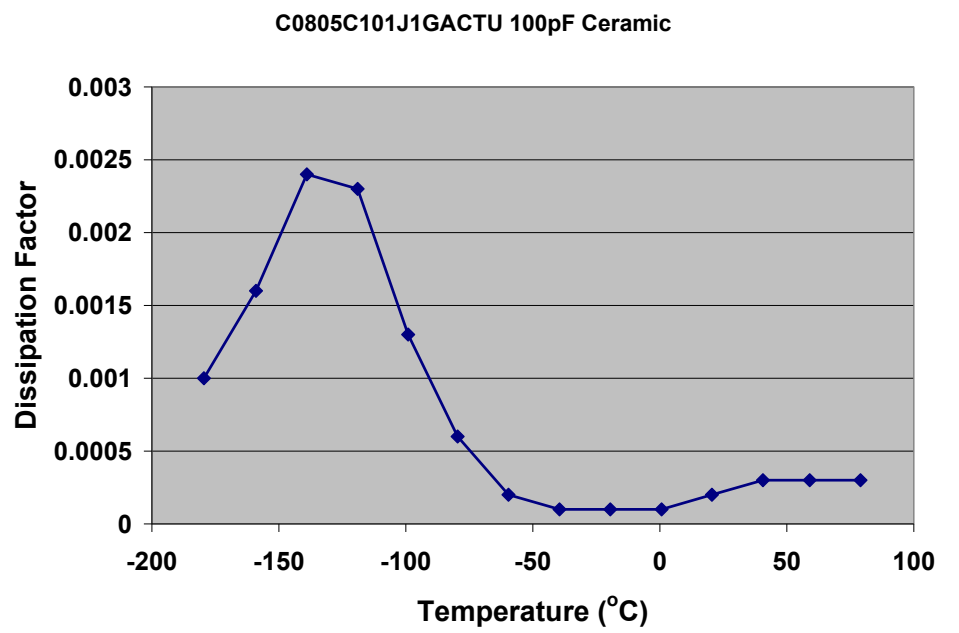


# Passive Components: 10Ω Thick Film Resistor

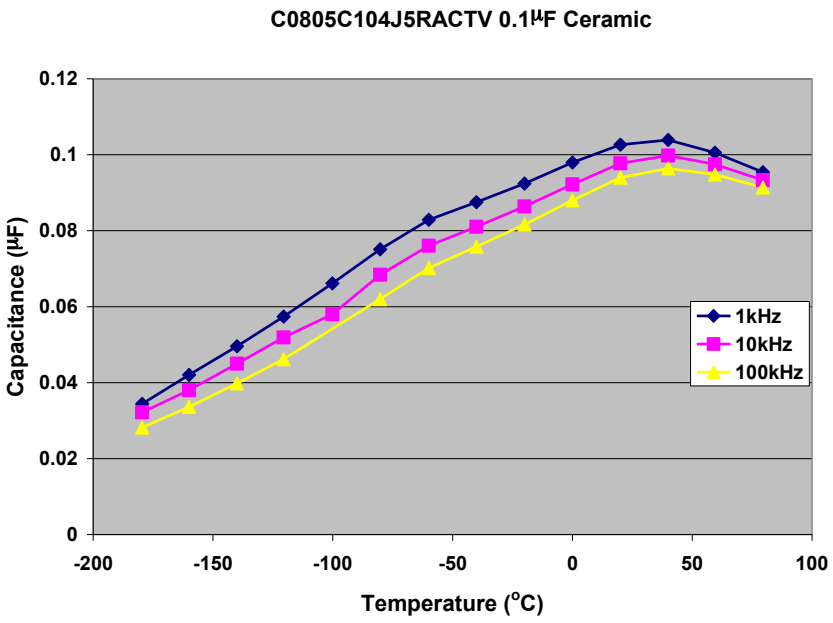


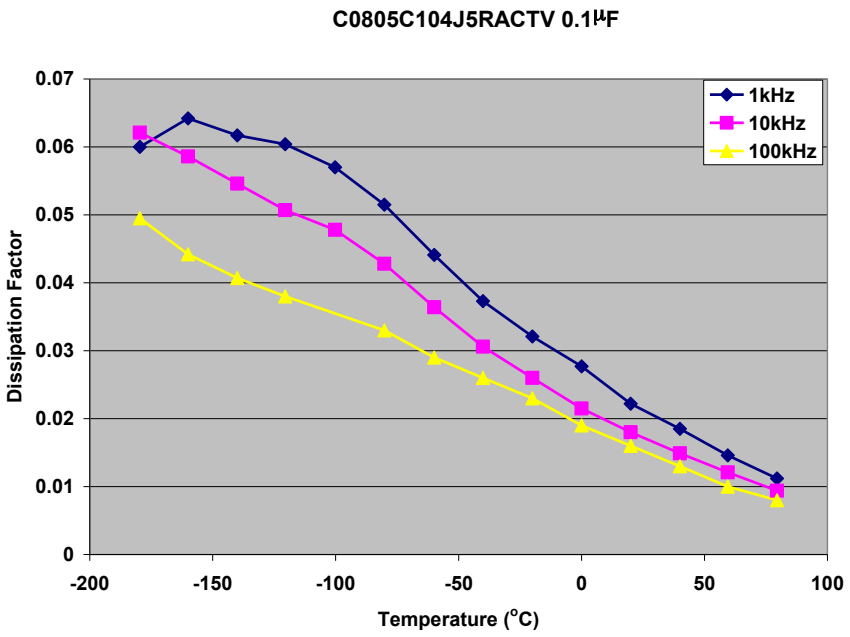
# Passive Components: 100pF NPO, 1MHz



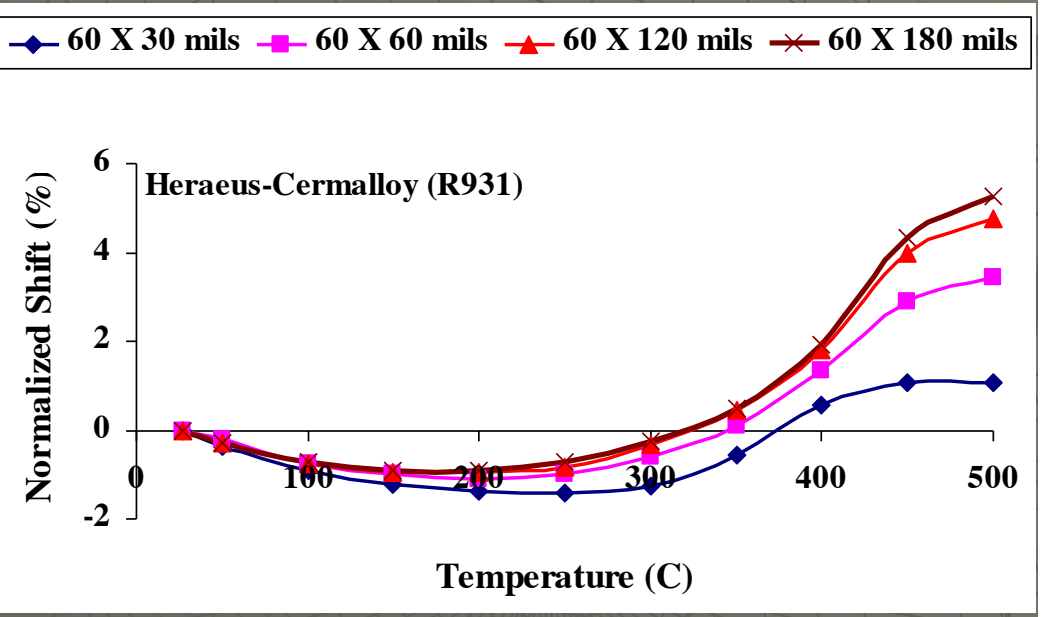



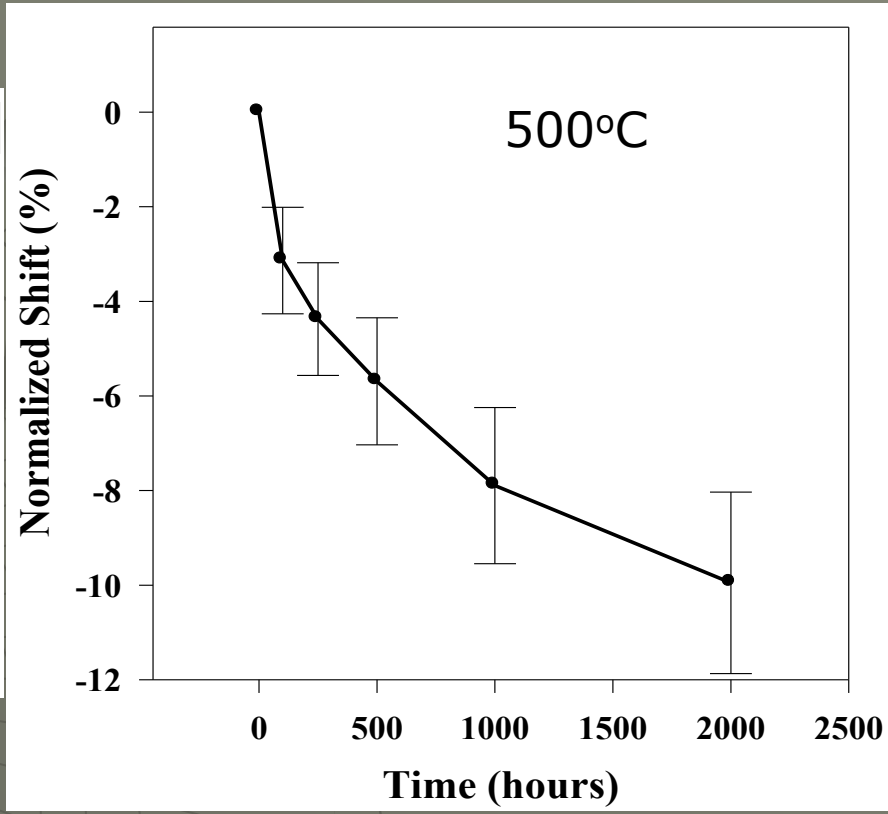
# Passive Components: 0.1μF X7R



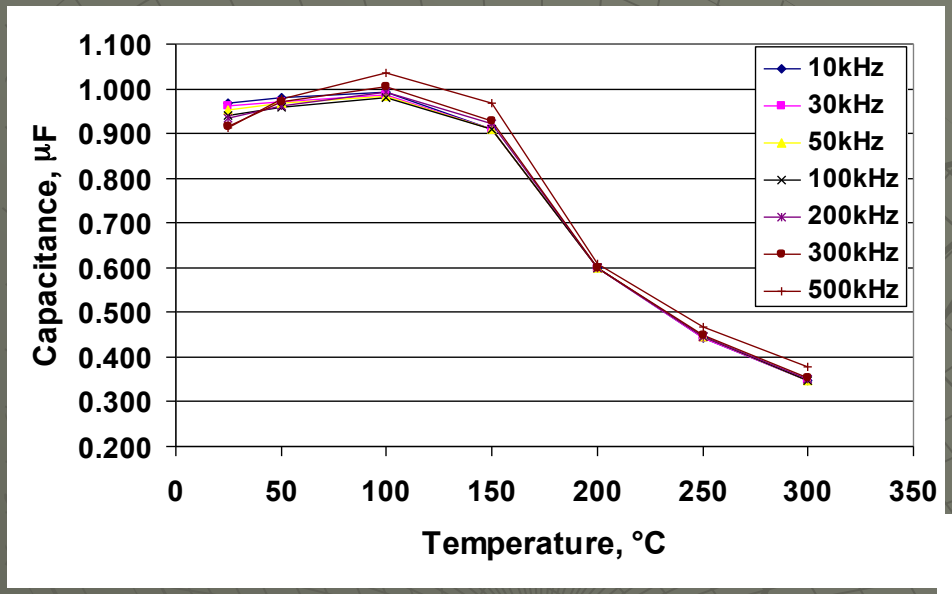



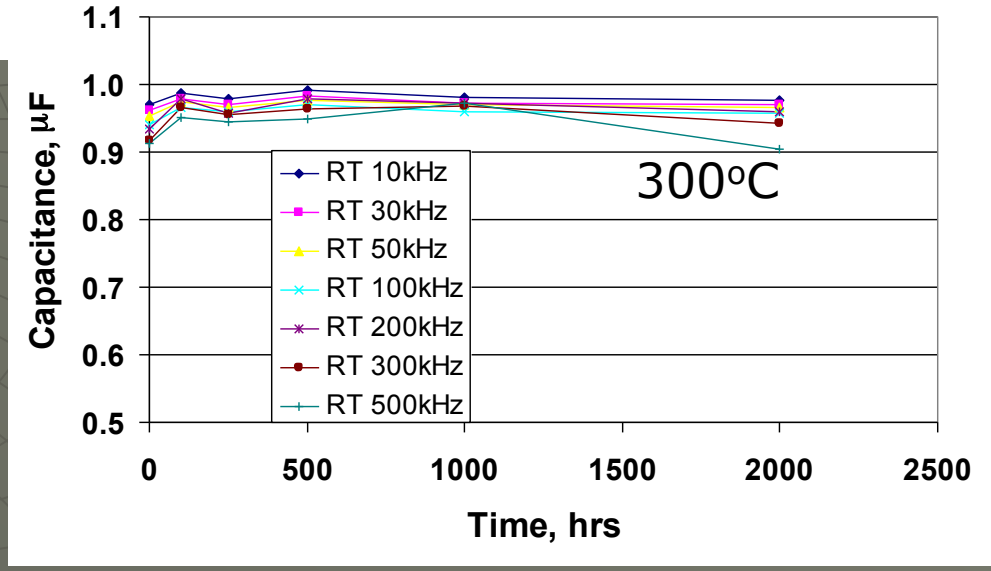
# Passive Components: Thick Film Resistors



# Passive Components: Capacitors

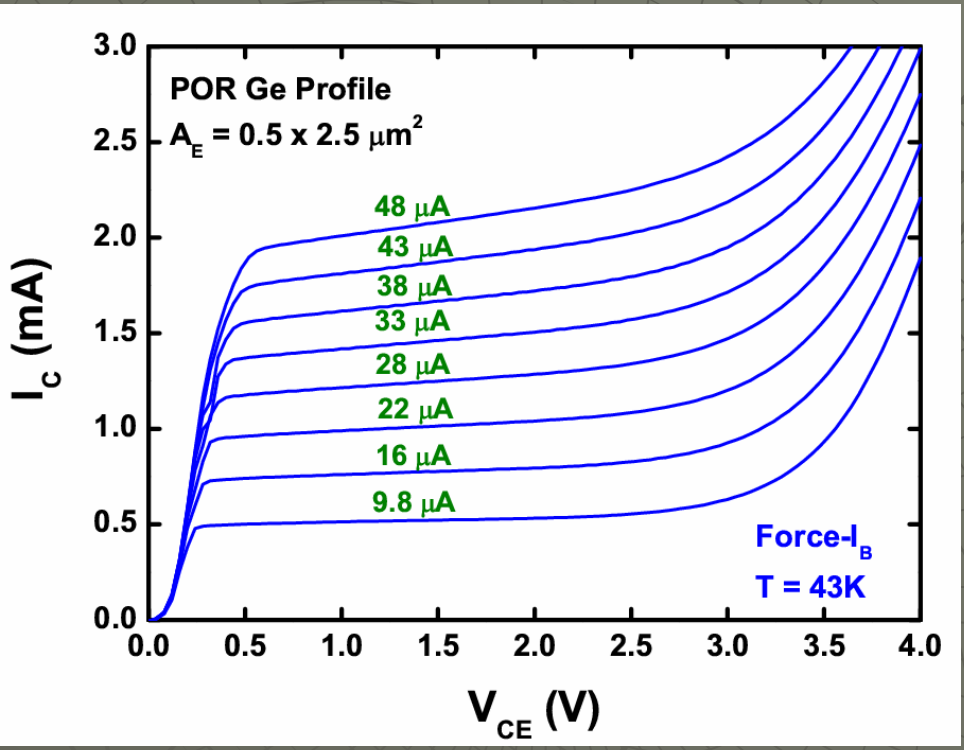


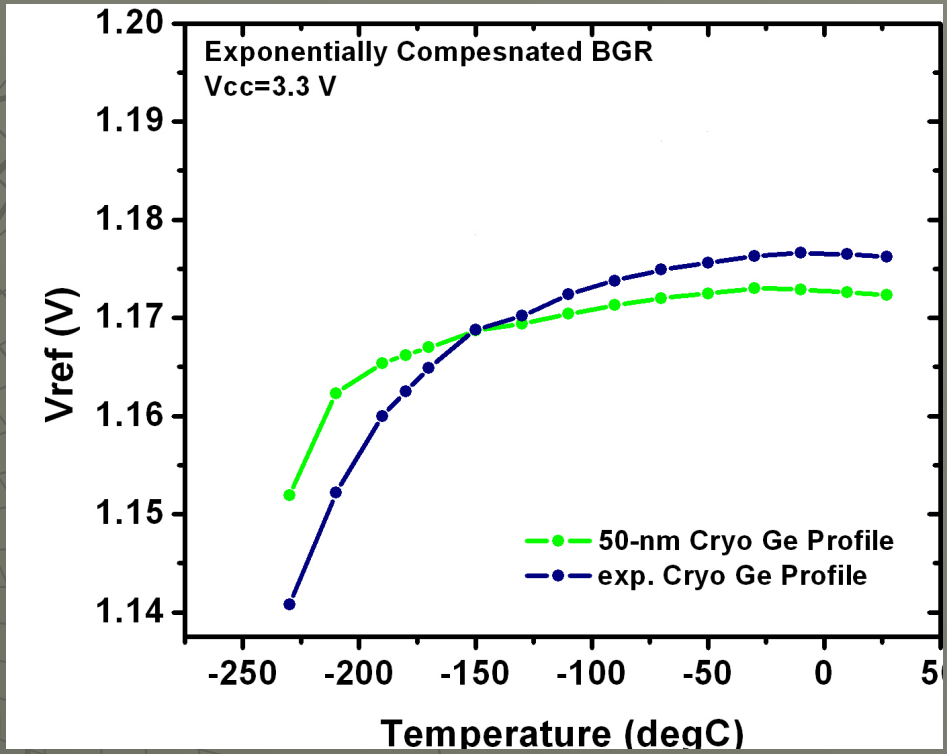



# Active Devices

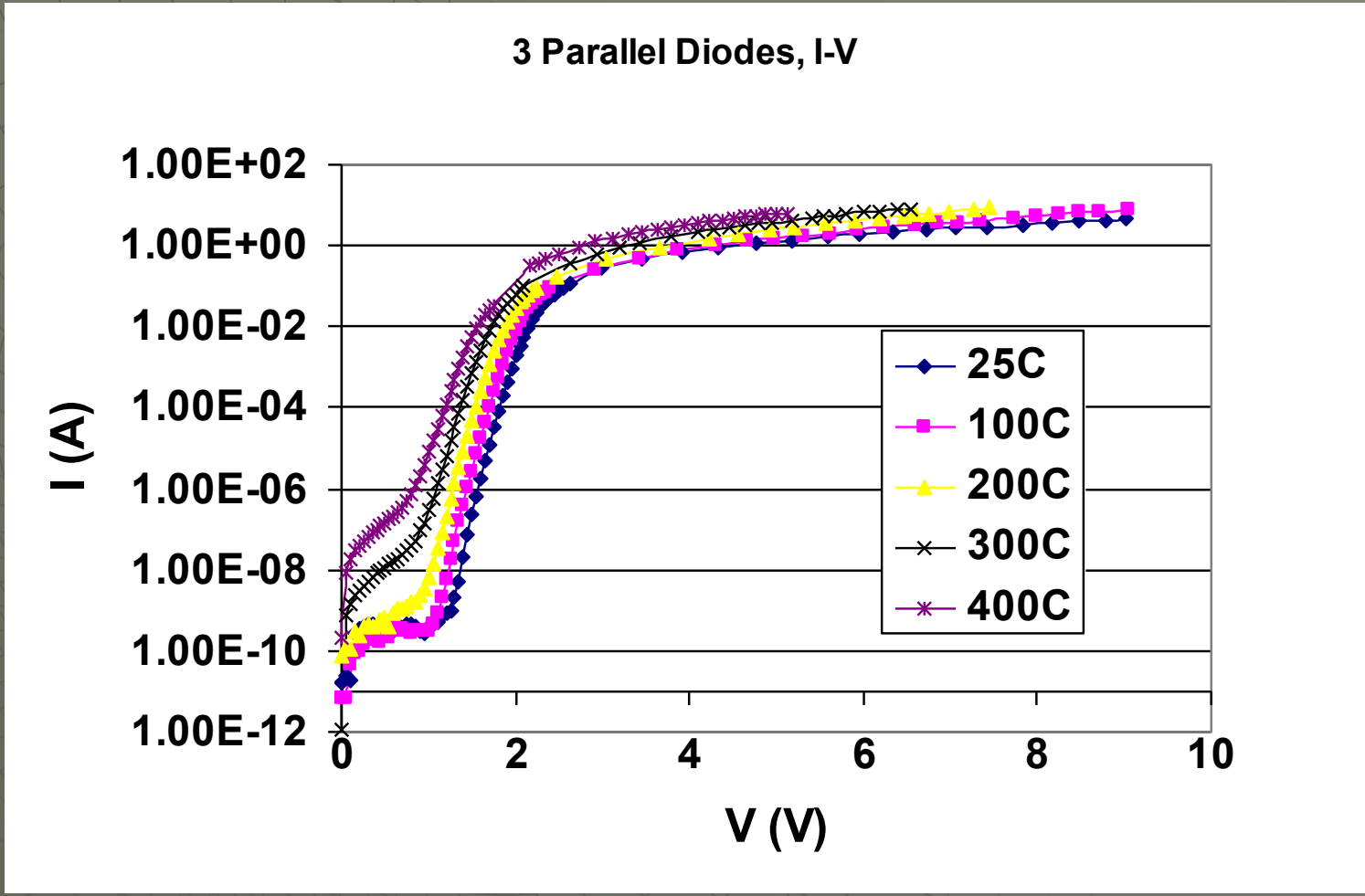
- Low Temperature
  - SiGe BiCMOS
- High Temperature
  - Silicon-on-Insulator
  - SiC
  - GaN

# SiGe


POR Ge Profile
$A_E$ = 0.5 x 2.5 μm²
48 μA
43 μA
38 μA
33 μA
28 μA
22 μA
16 μA
9.8 μA
Force-$I_B$
T = 43K
$I_C$ (mA)
$V_{CE}$ (V)
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0


Exponentially Compesnated BGR
Vcc=3.3 V
50-nm Cryo Ge Profile
exp. Cryo Ge Profile
Vref (V)
Temperature (degC)
1.14
1.15
1.16
1.17
1.18
1.19
1.20
-250
-200
-150
-100
-50
0

# SiC


3 Parallel Diodes, I-V
1.00E+02
1.00E+00
1.00E-02
1.00E-04
1.00E-06
1.00E-08
1.00E-10
1.00E-12
I (A)
0
2
4
6
8
10
V (V)
25C
100C
200C
300C
400C

# Packaging

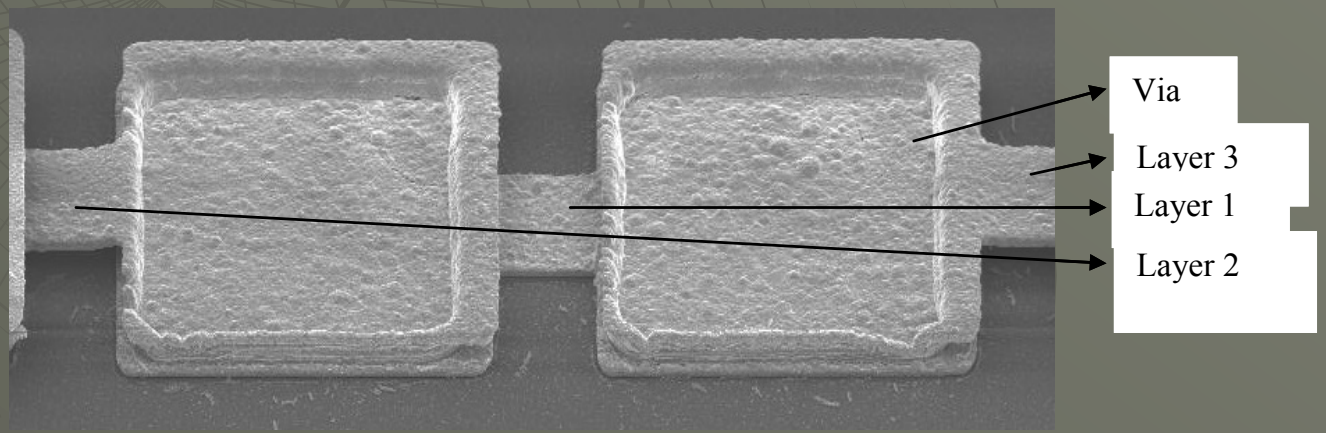
- Low Temperature
  - Static
    - Material property changes
  - Cycling
    - Fatigue
      - CTE mismatch
    - Creep at high temp
    - Diffusion, intermetallics and grain growth at high temp
- High Temperature
  - Static
    - Limited materials
    - Material property change
    - Diffusion, intermetallics and grain growth
    - Creep
  - Cycling
    - Fatigue
    - Creep

# Low Temperature Packaging

- Multichip module approach
  - Reduced size and weight
  - Reduced number of interfaces
- Attempt to match Coefficients of Thermal Expansion (CTE's)

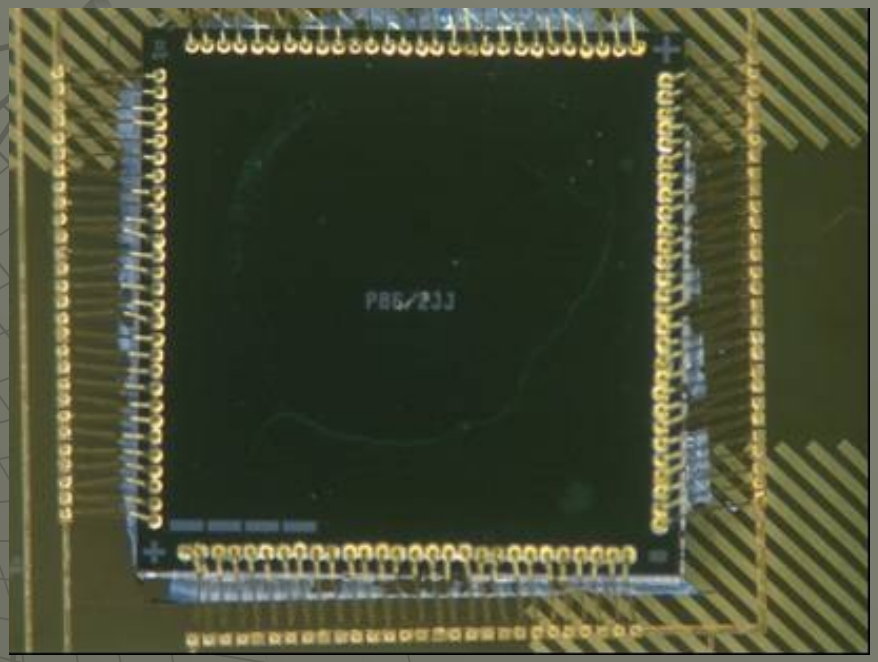
# Low Temperature Packaging

- Substrates
  - AlN for wire bond
  - Si or $Si_3N_4$ for flip chip
- Multilayer interconnect
  - Polyimide PI-2611
  - Cu
    - Ni/Au pad finish for wire bonding and flip chip



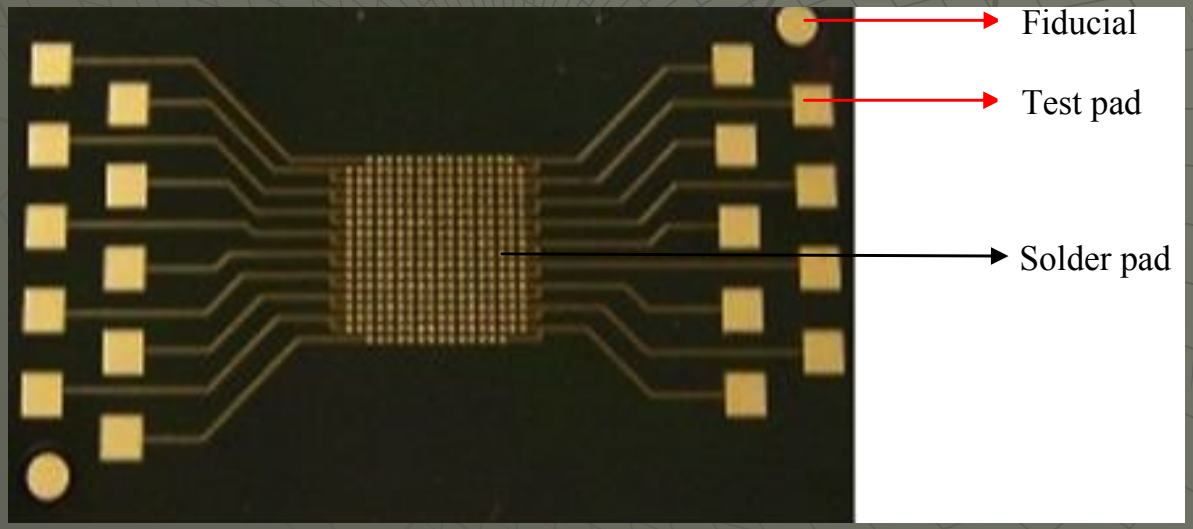
# Low Temperature Packaging

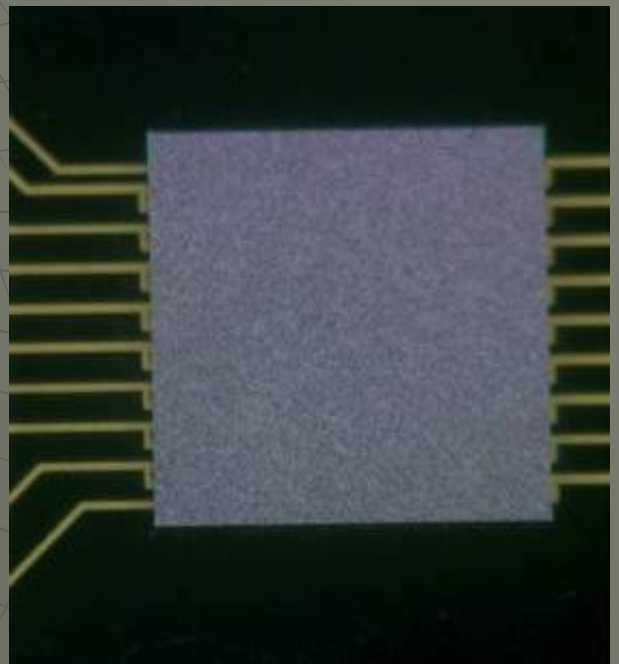
- Wire bond
  - In die attach
    - Custom backside metallization
      - 50 liquid thermal shock cycles, -196°C to +125°C, No die attach failures
  - Au thermosonic wire bonding



# Low Temperature Packaging

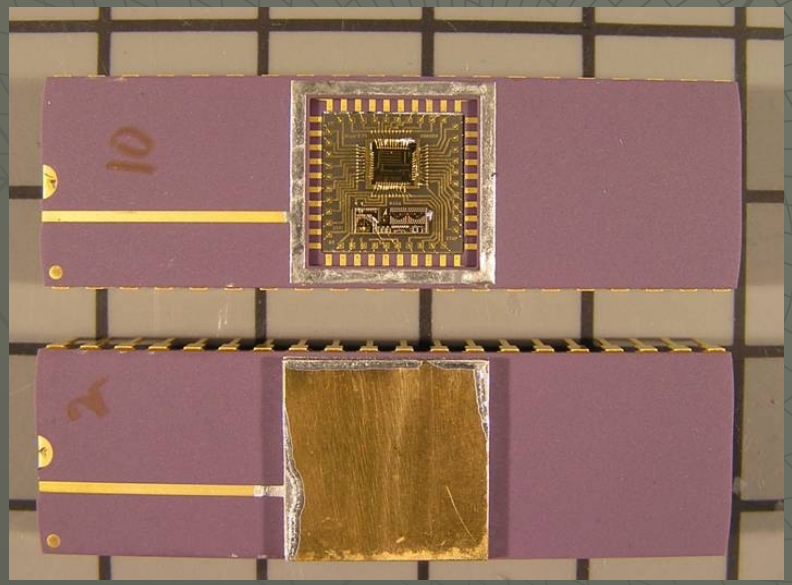
- Flip chip
  - In/Pb (50/50) solder bumps
  - No underfill
    - 50 liquid thermal shock cycles, -196°C to +125°C, No failures

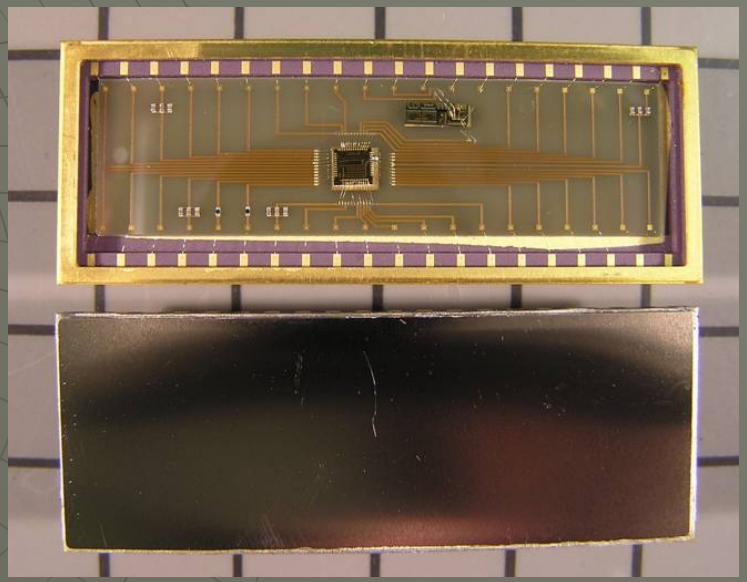


# Low Temperature Packaging

- $Al_2O_3$ ceramic packages
  - In substrate attach
  - SnPb eutectic solder seal
    - 50 liquid thermal shock cycles, -196°C to +125°C, No substrate or lid seal failures

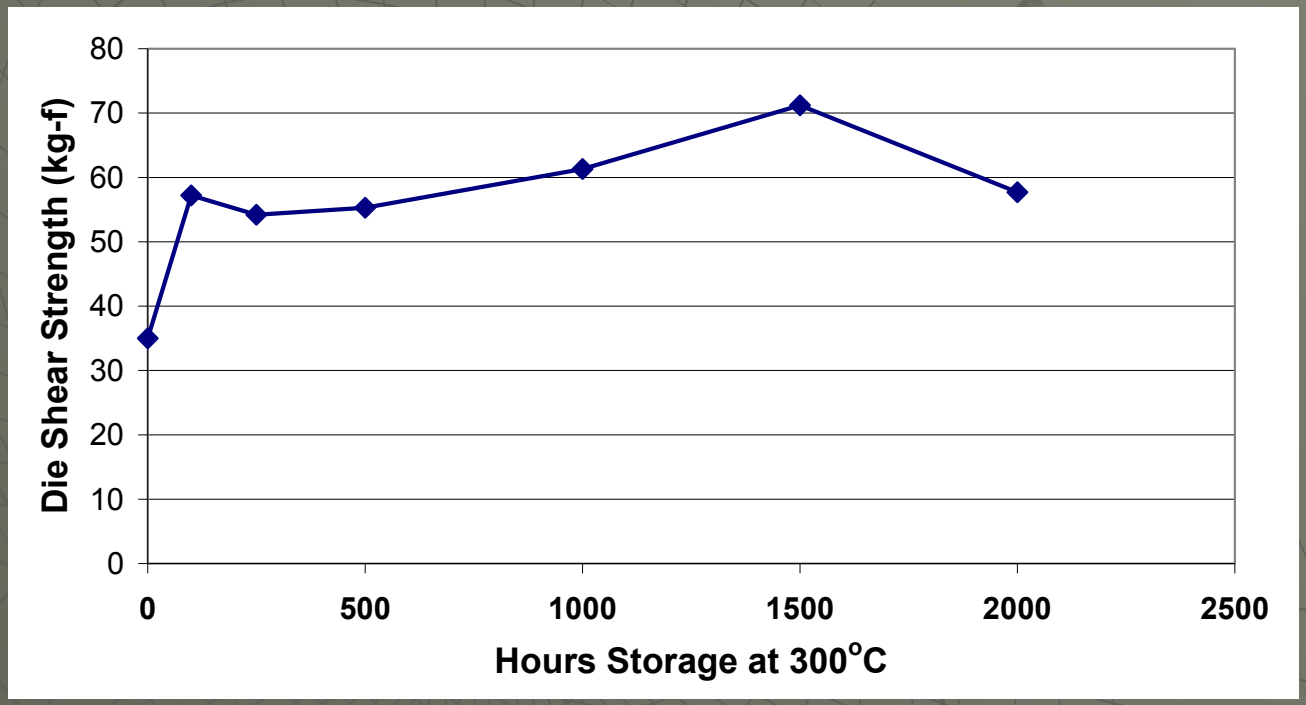




# High Temperature Packaging

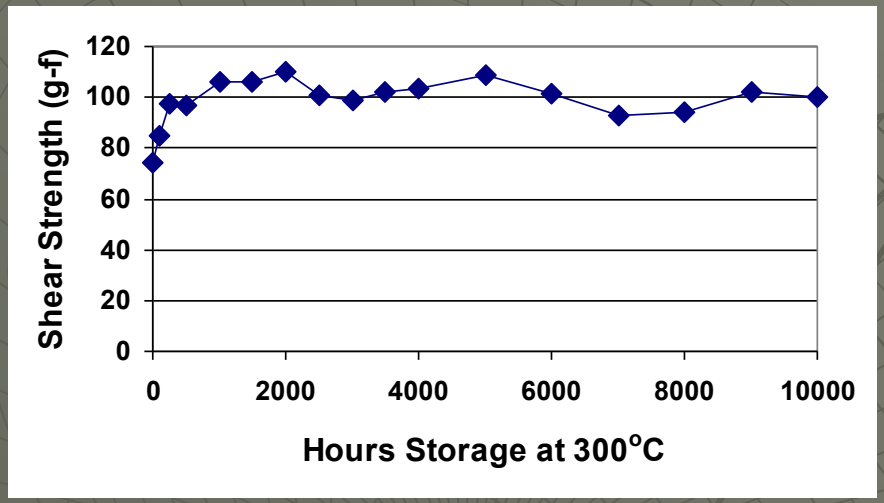
- SOI
  - $\leq 300^{o}C$
    - Die attach
    - Wire bonding
- SiC
  - $\geq 300^{o}C$
    - Die attach
    - Wire bonding

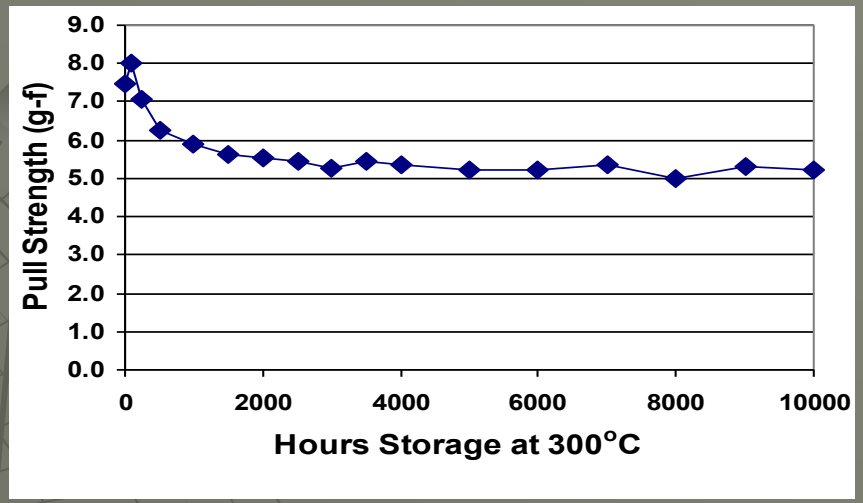
# AuGe Die Attach on Thick Film $Al_2O_3$ Substrate

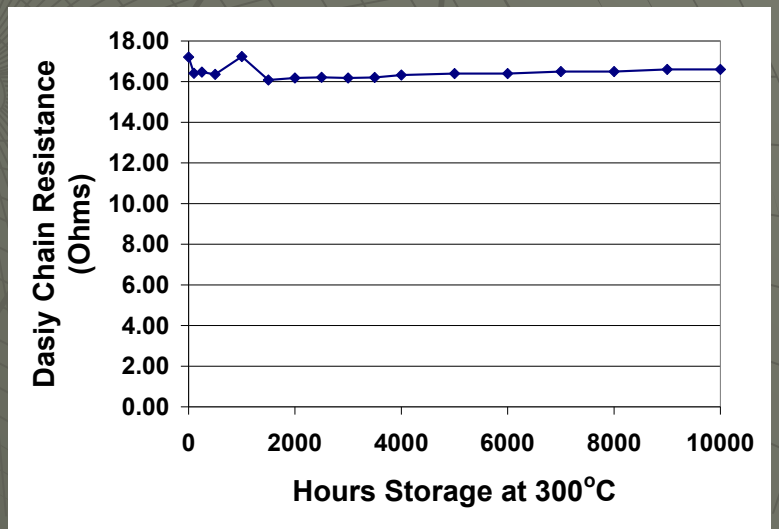



5mm x 5mm die attached to an Al2O3 substrate metallized with DuPont 5771 thick film Au

# Wire Bond with Electroless Ni/ Electroless Au over Al Wire Bond Pads

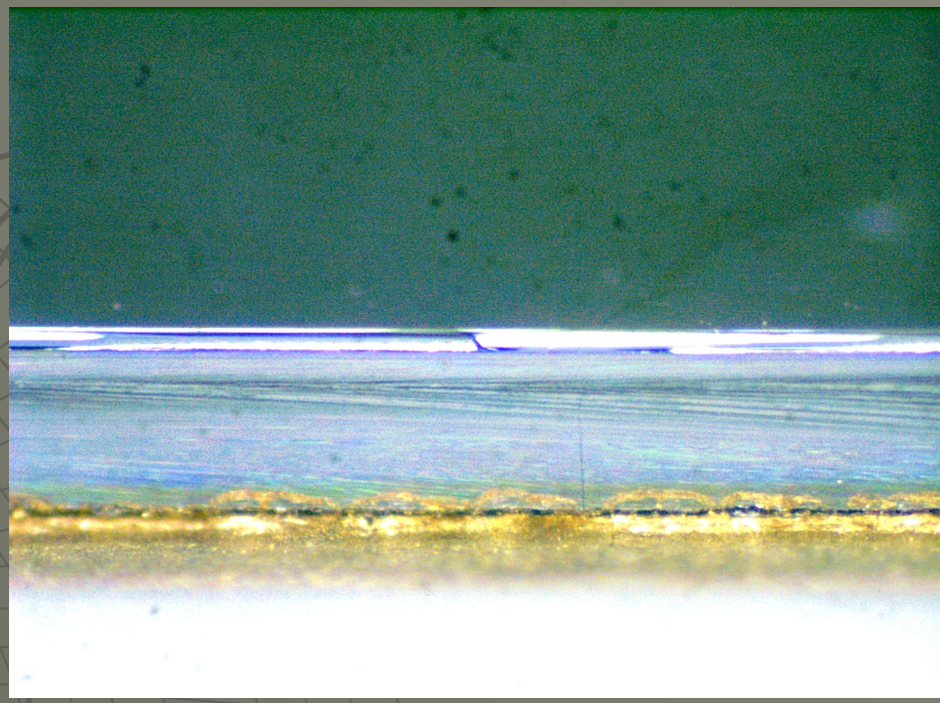


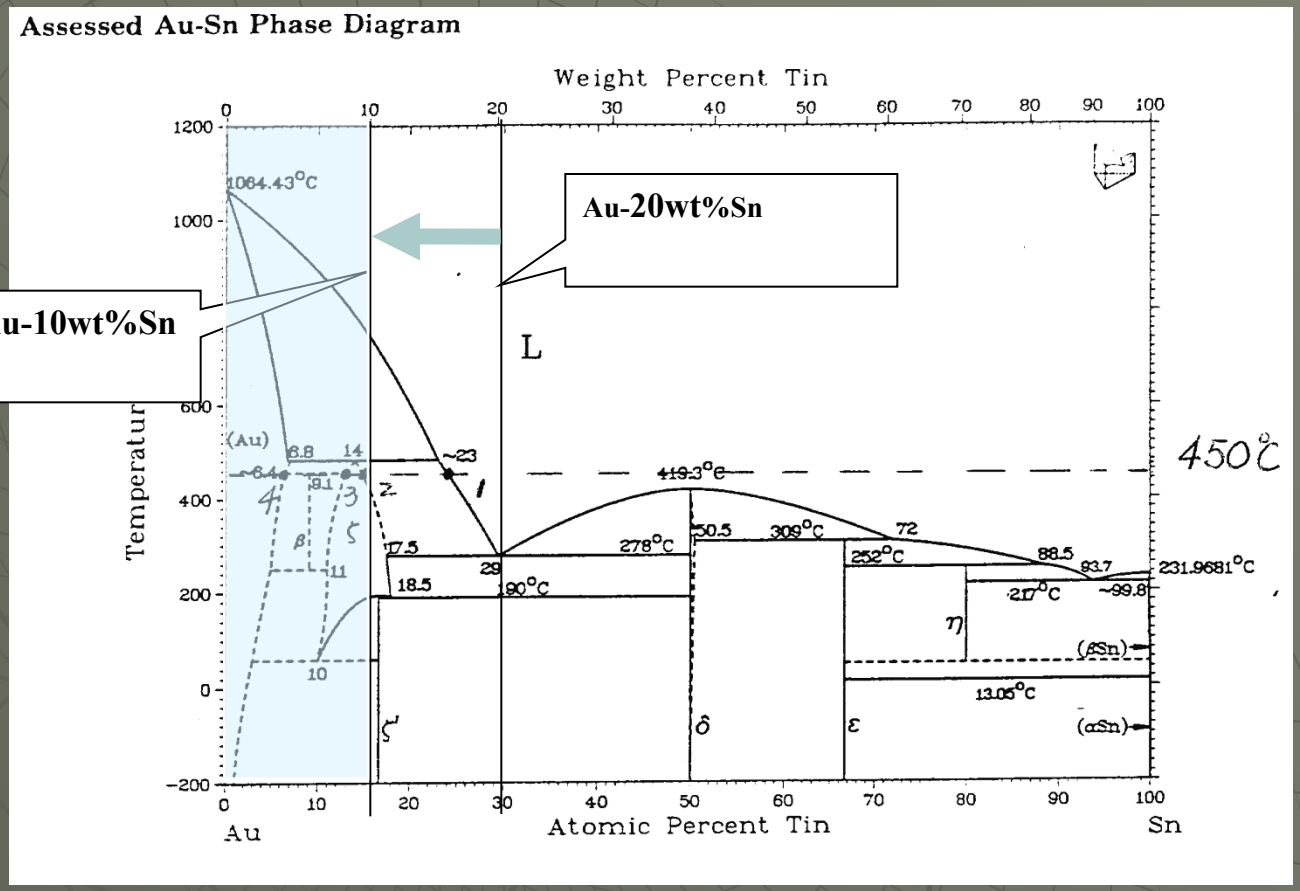
# Thermal Cycling

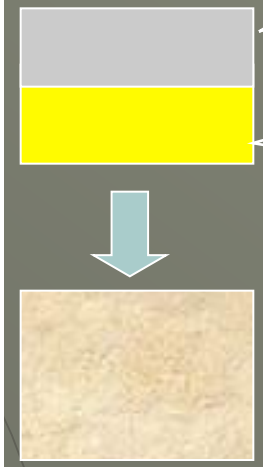
- $Al_2O_3$ ceramic substrate
- Thick film metallization
- AuGe die attach
- 5mm x 5mm Si die
- +40°C to 300°C



500 cycles

# SiC Die Attach: Au-Sn Bonding Process



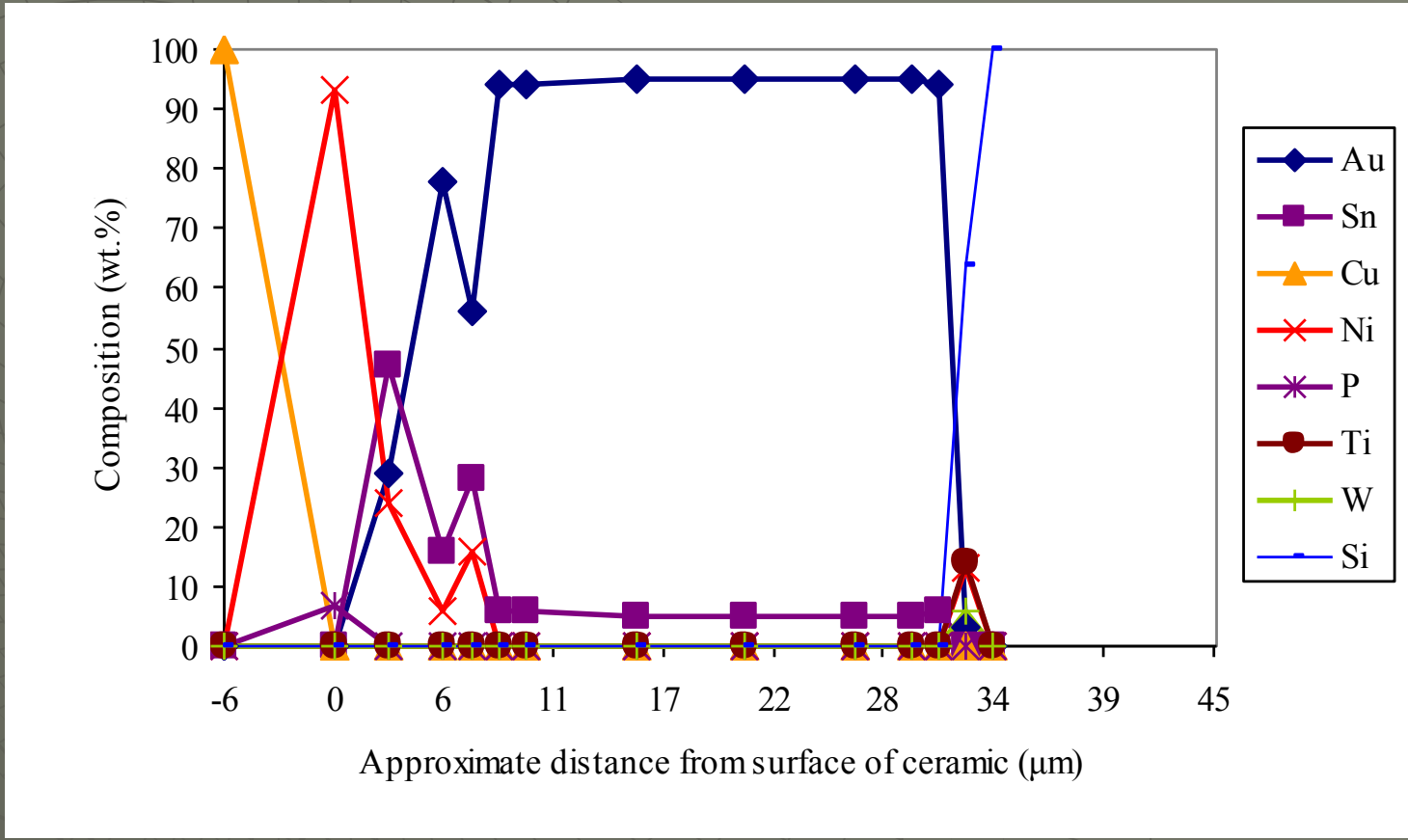



Au-20wt%Sn
Tm=280°C

Au
Tm = 1064°C

Au-<10wt%Sn
Tm~450°C

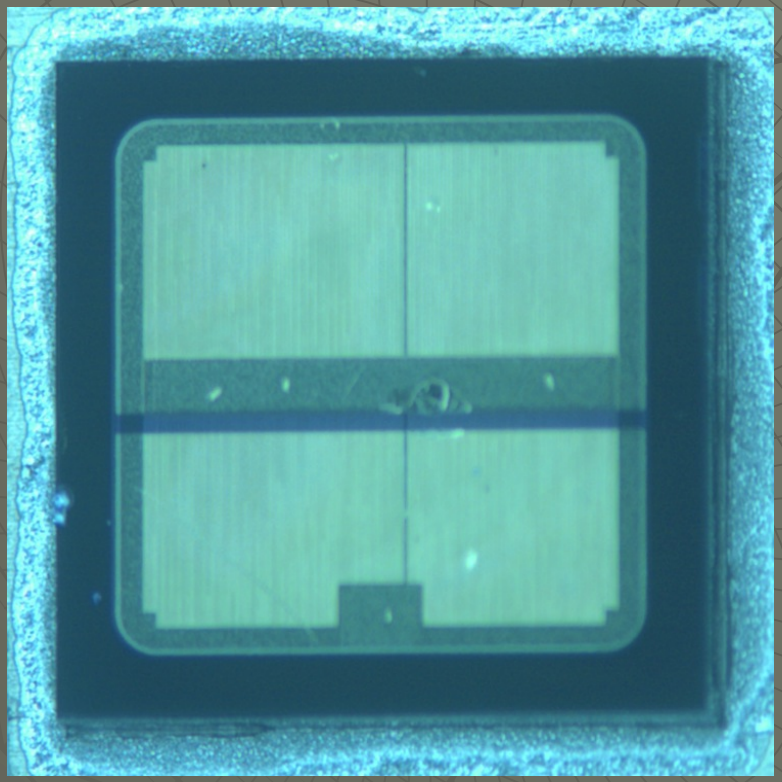
# EDS Line Scan of Braze Cross Section: Achieved Sn <10%

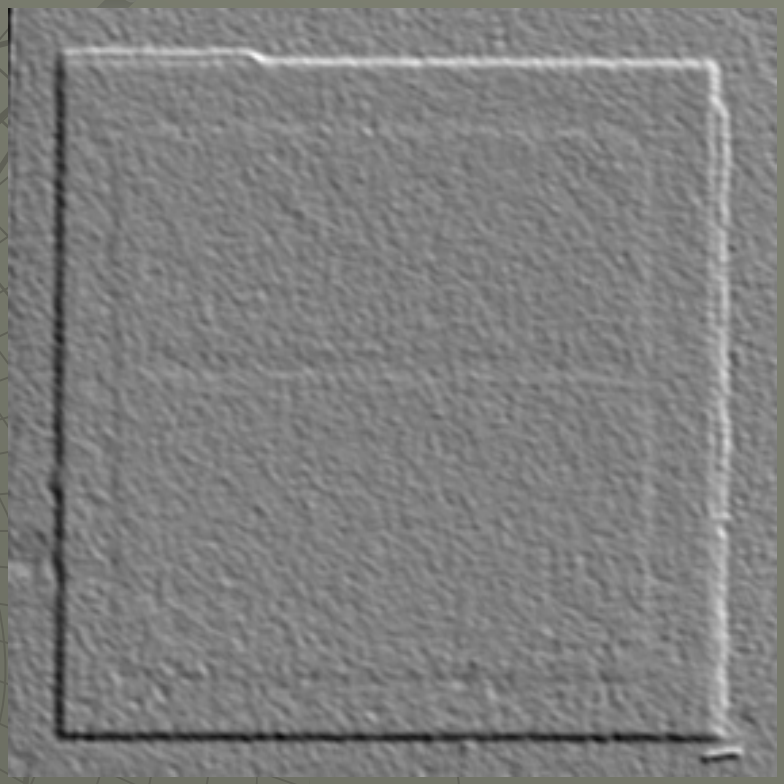



Substrate

SiC Die

# Optical and X-ray Images of Attached Die

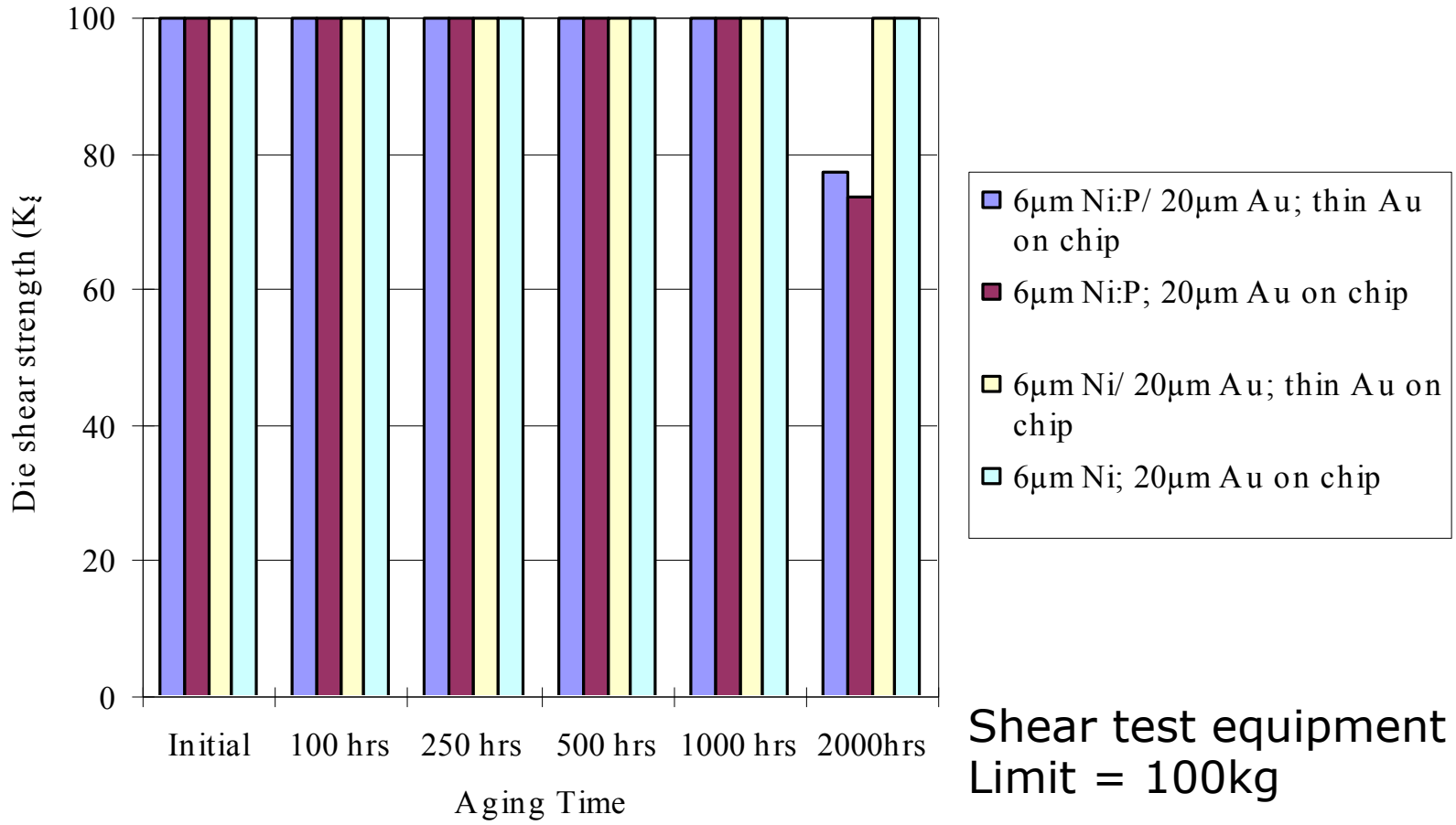




# Au-Sn Reliability

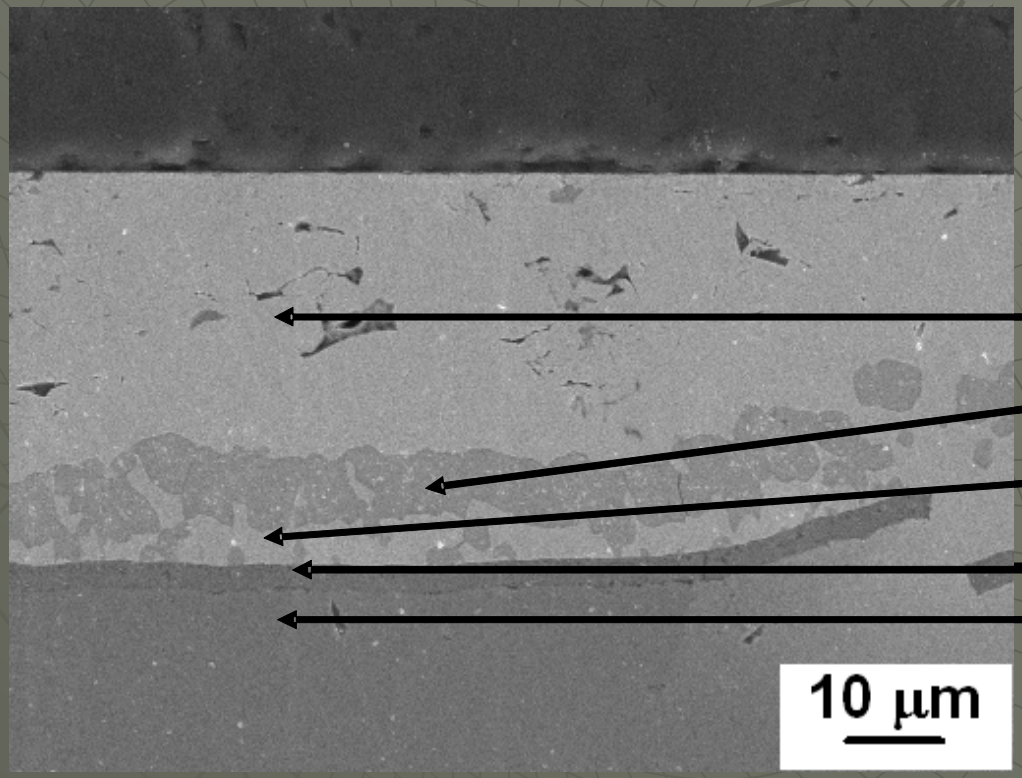
- Substrate: Cu/Ni/Au DBC
- Die size = 3.8mm x 3.8mm
- SiC pad stack: $NiSi_2$/Ti/Ti-W/Au
- Test combinations:
  - DBC on $Al_2O_3$ with electroless Ni:P, thick Au (20μm) on substrate
  - DBC on $Al_2O_3$ with electroless Ni:P, thick Au (20μm) on chip
  - DBC on $Al_2O_3$ with electrolytic Ni, thick Au (20μm) on substrate
  - DBC on $Al_2O_3$ with electrolytic Ni, thick Au (20μm) on chip

# Die Shear Strength after Aging at 400°C




Shear test equipment Limit = 100kg

# Cross Section of AuSn brazed sample after 2000 hours storage at 400ºC, electroless Ni:P, thick Au on chip




All compositions are in weight percent

90%Au, 9%Cu, 1%Sn

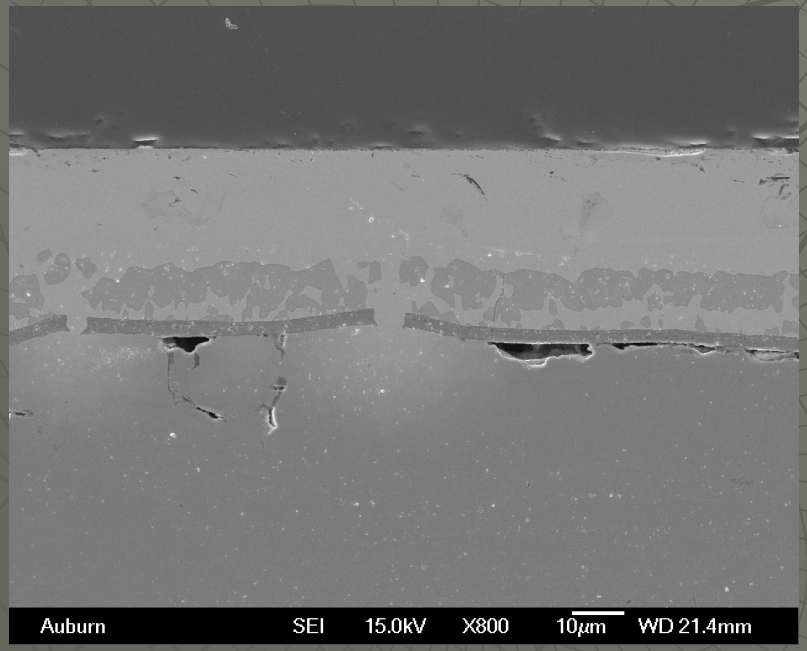
52%Sn, 32%Ni, 16%Au

87%Au, 13%Cu

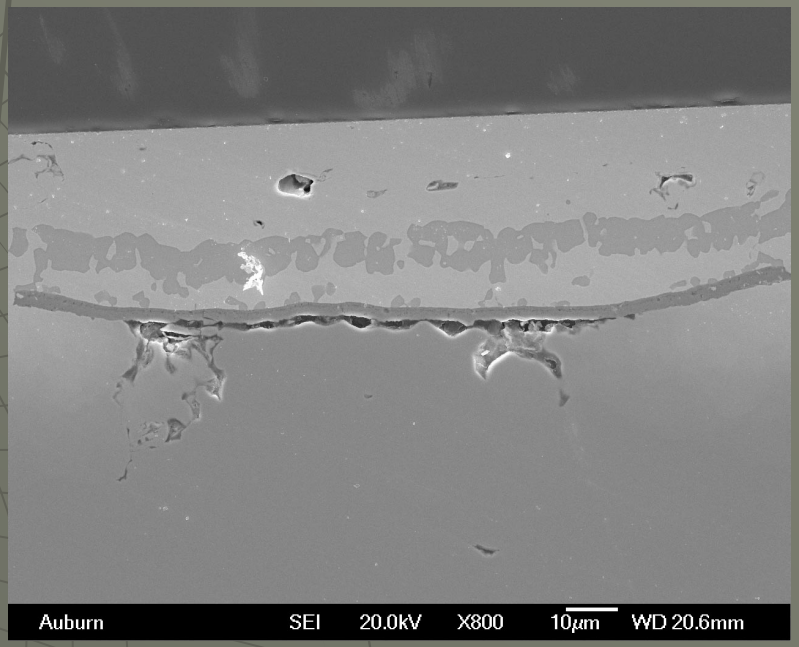
82%Ni, 15%P, 3%Cu

100%Cu

# Cross-section of the Die Attach: Voids at Cu-Ni:P interface after aging at 400ºC

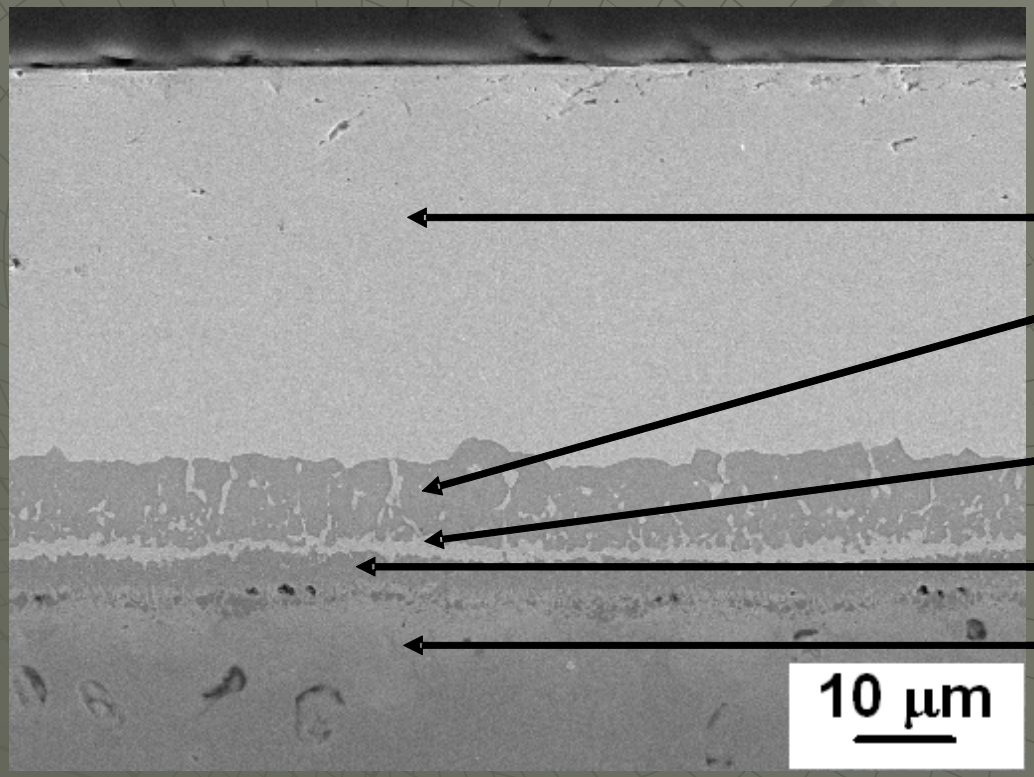



1000 Hours Aging




2000 Hours Aging

# Cross Section of AuSn brazed sample after 2000 hours storage at 400ºC, electrolytic Ni, thick Au on substrate




All compositions are in weight percent

97%Au, 3%Cu

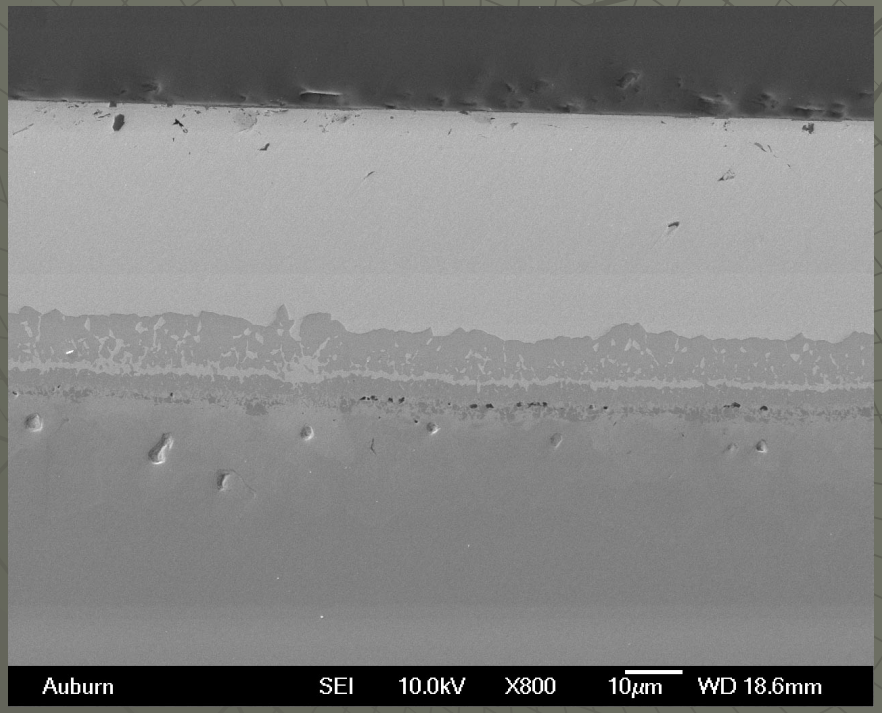
53%Sn, 35%Ni, 12%Au

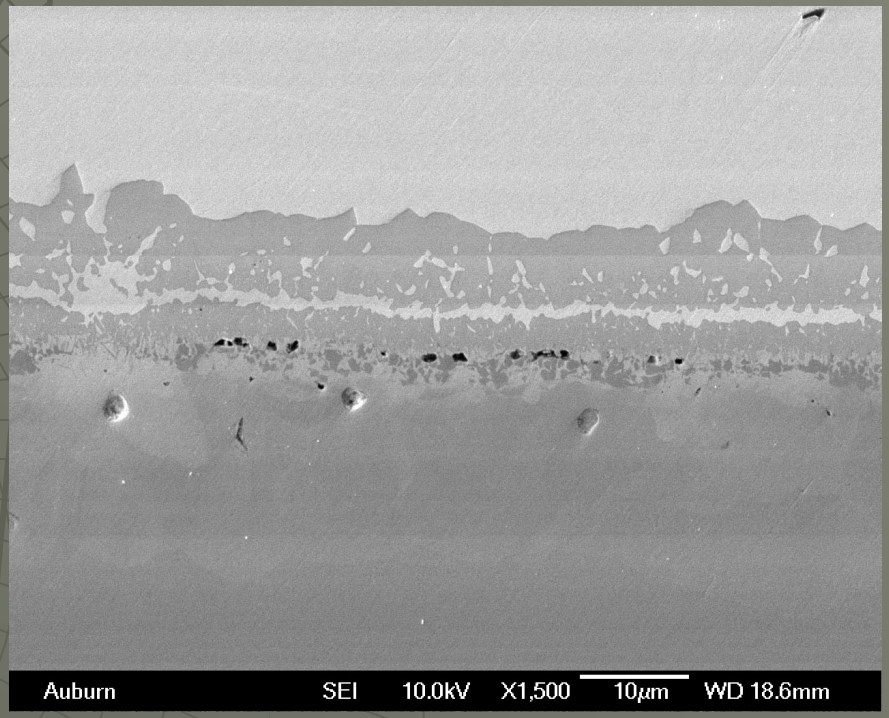
72%Au, 26%Cu, 2%Ni

55%Ni, 41%Sn, 4%Cu

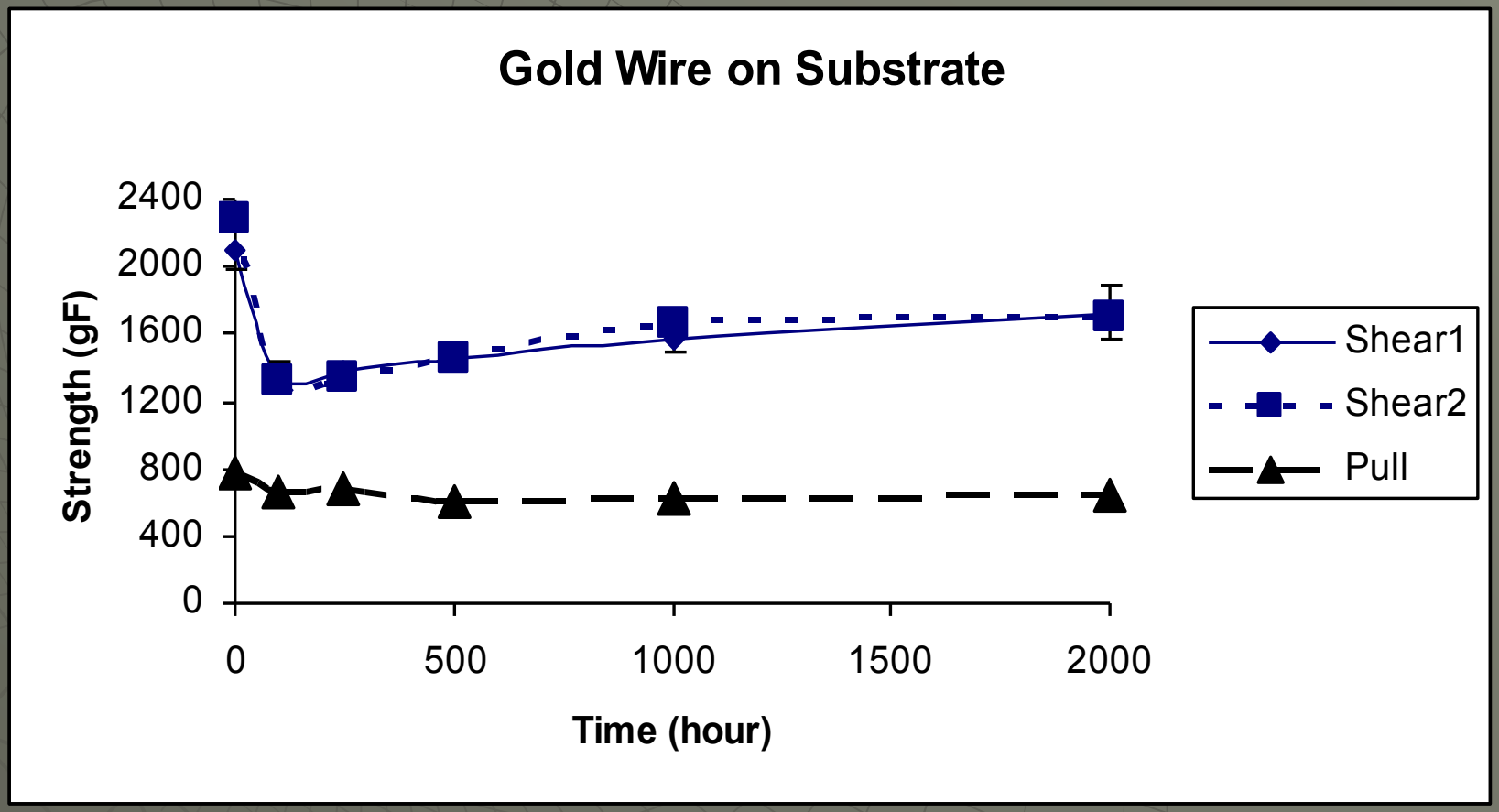
32%Cu, 28%Ni, 26%Au, 14%Sn

# Cross-section of the die attach, showing limited voiding at Cu-Ni interface after 2000 hours aging at 400ºC

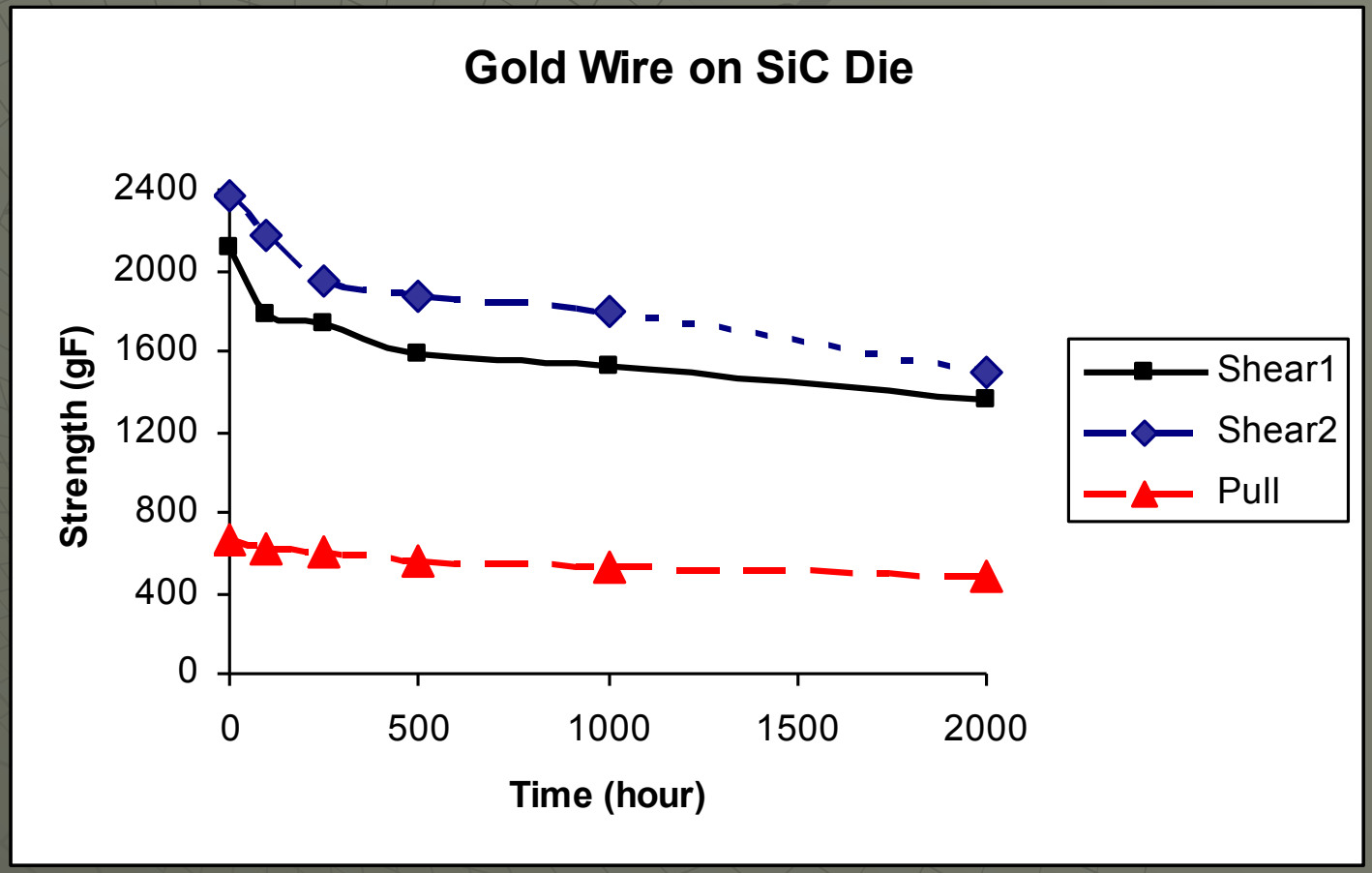


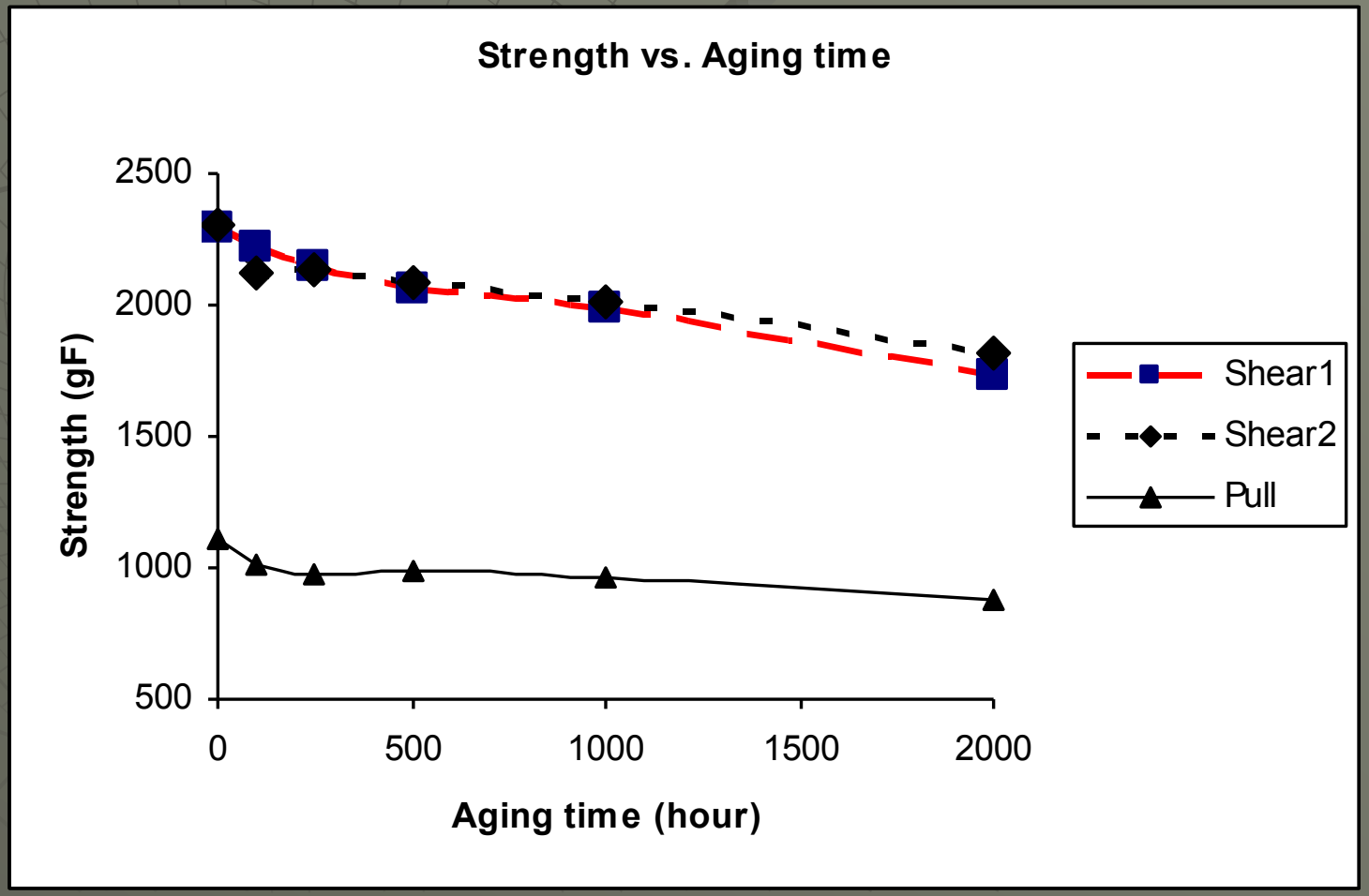
# Wire Bonding: Au Wire & Cu/Ni/Au Metallization on Ceramic Substrate



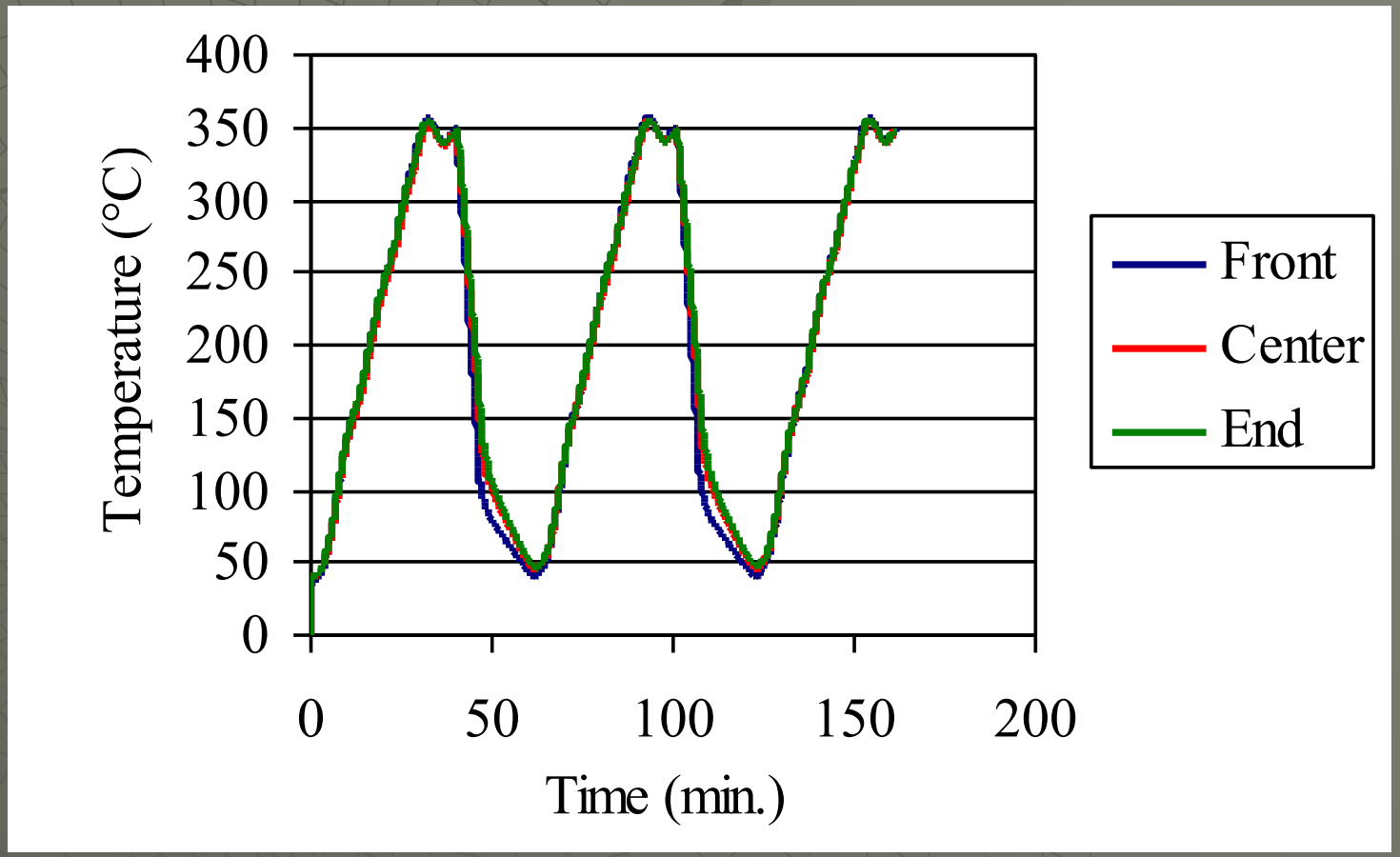
# Wire Bonding: Au Wire & Ti/Ti:W/Au Pads over $SiO_xN_y$ Passivation



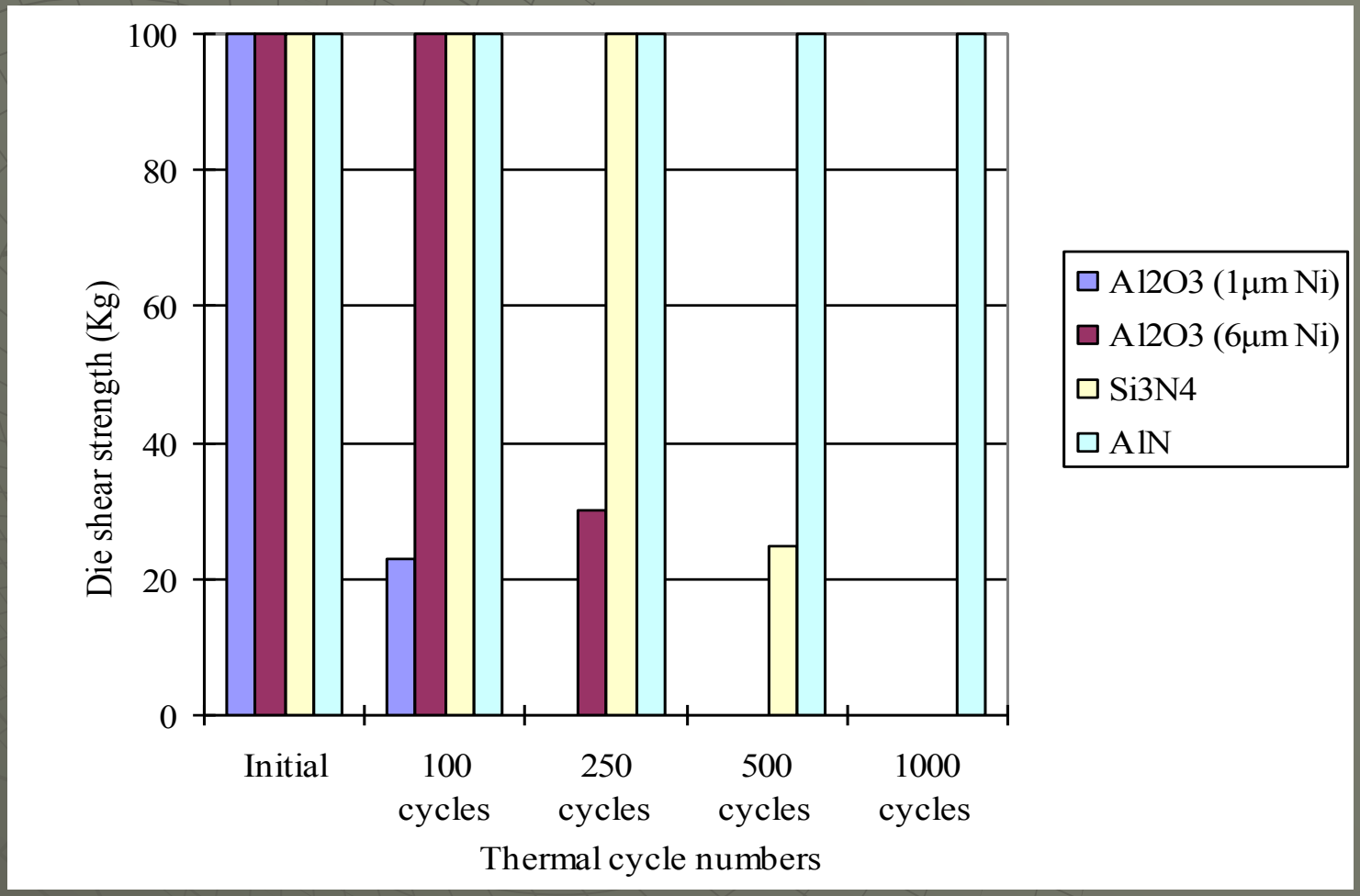
# Au Wire Bonding: 350°C Aging on Ta:Si:N (2%) / Pt:N(2%)/Au on nickel silicide



# Thermal Cycle: Profile



# Thermal Cycle: Results for Different Power Substrates

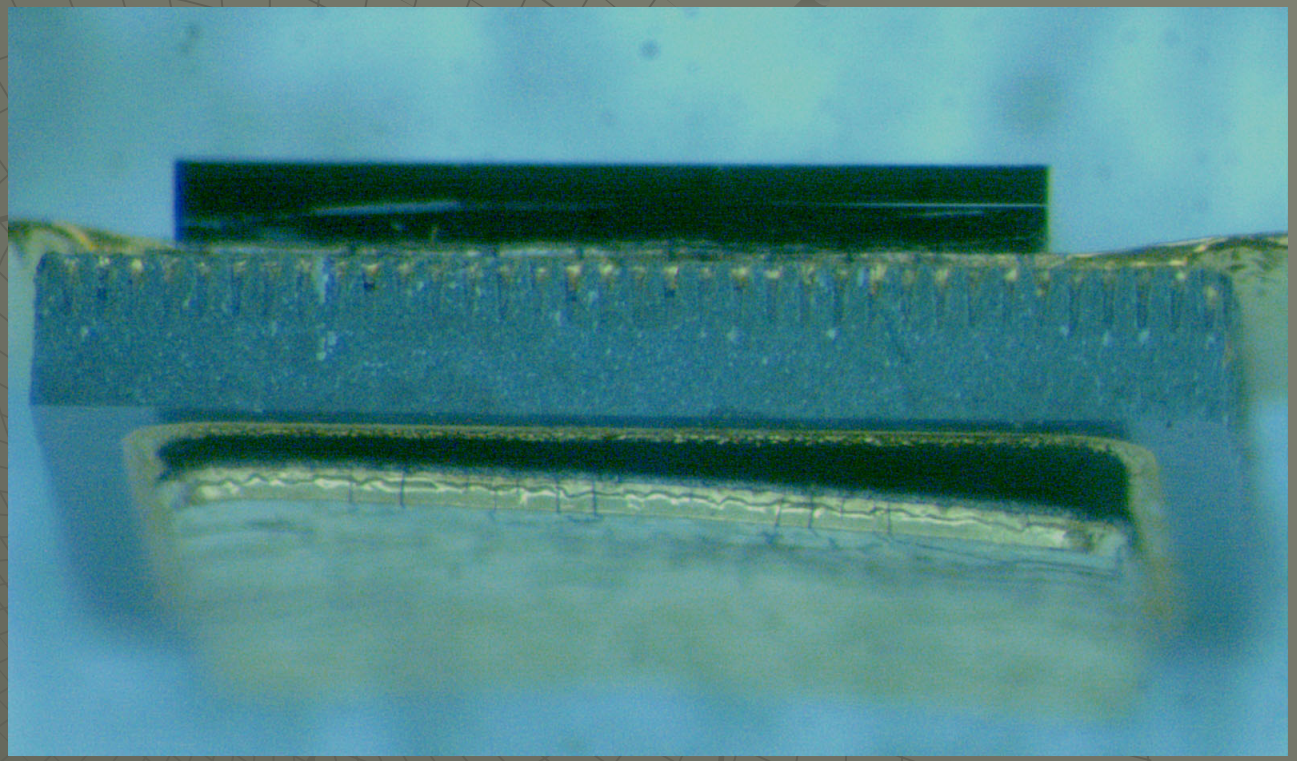


# Thermal Cycles: DBC $Al_2O_3$ Observations

- After 100 thermal cycles Cu foil had started to delaminate from DBC $Al_2O_3$ with 250µm Cu
- After 250 thermal cycles Cu foil had started to delaminate from DBC $Al_2O_3$ with 190µm Cu

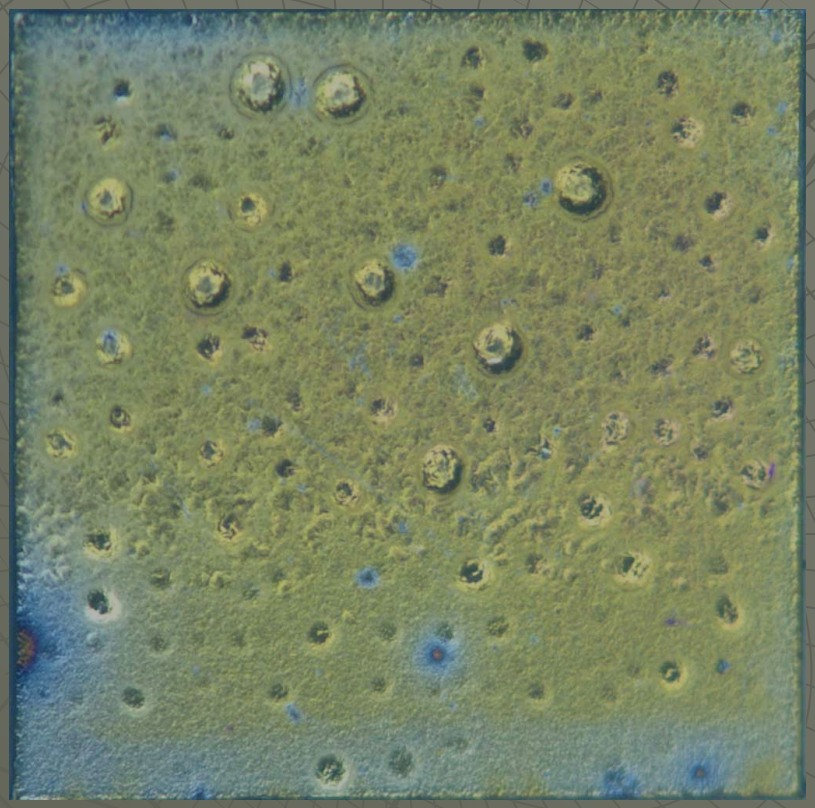
DBC $Al_2O_3$ with 190µm Cu after 250 thermal cycles
Failure in upper surface of $Al_2O_3$

# Thermal Cycles: $Si_3N_4$



Cu (154μm) delamination after 500 cycles
Fracture is in the surface of the $Si_3N_4$

# Thermal Cycling: AlN



After 100 cycles

**Blisters were observed in Cu (45μm) layer after 100 thermal cycles**

**Only o ccurred on one side: Implies adhesion layer/ plating issue in fabrication**

**Die shear strength remained high**

# Summary

- Device and packaging technologies are being developed for extreme environment applications in space
- Passive and active devices are available
  - Performance as a function of temperature must be considered in design
  - High temperature reliability of SOI must be considered

# Summary

- A multichip module approach to low temperature electronics packaging is being developed
  - Both static and cycling applications
- High temperature packaging has been demonstrated for static applications at 300$^{o}$C
  - Extendable to 500$^{o}$C
  - Significant challenges exist for cyclic applications

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