Electronics Packaging for Extreme Environments

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ABSTRACT

Space exploration encompasses a wide range of environments in which it would be desirable to operate electronics for control, sensing, communications and actuation. However, most electronics are designed to operate in earth-like environments. Thus, the current approach is to provide an earth-like environment for space electronics. This includes 'warm boxes' for cold environments and dewars for limited operating life in high temperature environments. This adds to system weight, complexity and energy consumption. New device technologies such as silicon-on-insulator, silicon-germanium, silicon carbide and gallium nitride are making possible electronic devices capable of operating over very wide temperature ranges. In this paper, device technologies are first reviewed. Then the challenges and opportunities for packaging these devices for operation directly in the ambient environment are discussed.

INTRODUCTION

Space exploration provides a number of examples of extreme environments. In the equatorial region of the moon, the temperatures range from -180°C (night) to 120°C (day), while in the permanently shadowed craters the temperature remains at -230°C. While radiation exposure is low, 100krad, solar activity creates potential for radiation induced single event effects. The Mars environment is -120°C to +85°C with radiations levels of 300krad. At the other environmental extreme is Venus with a surface temperature of 485°C and a pressure of 90 bars.

Distributed electronics able to operate in the ambient lunar and Martian environments are necessary to enable the lunar/Martian vision of habitats, rovers, mining and manufacturing, orbiting vehicles, etc. The current small-scale Mars rovers, Spirit and Discovery use warm electronics boxes to maintain the electronics in an earth-like temperature environment. This results in over 2000 point-to-point wires, increasing system complexity and weight. It also increases challenges in system test and debug prior to launch. This centralized approach will be limiting as larger vehicles are needed. For intelligent, distributed sensors and actuators, the electronics and sensors must operate in the ambient environment.

Thermal protection systems, dewars, phase change materials, etc., can be used to decrease the rate of temperature rise for electronics that land on the surface of Venus. However, in a mission targeted for 90 days on the Venus surface the electronics will eventually reach 485°C and conventional electronics will fail long before that time. Increasing the operating temperature capability of the electronics will increase the operating life of the probe and/or reduce the size and weight of the probe by reducing the complexity of the thermal protection system.

This paper explores the challenges and opportunities for electronics capable of operating in the ambient environment. The focus will be on the effects of temperature extremes.

DEVICE TECHNOLOGY

Electronic systems include a combination of passive (resistor, capacitor, inductor) and active (diodes, transistors, integrated circuits) devices to performed the desired sense, compute, communicate and actuate functions. The key challenges in extreme temperature devices are the changes in operating parameters as function of temperature and the reliability of the device.

Passive devices – Examples of the effect of temperature on the electrical characteristics of commercially available resistors and capacitors are shown in Figs. 1-4. In the case of the resistors (Figs. 1 and 2) and the NPO capacitor (Fig. 3) the change in value over the temperature range is not large. However, the larger capacitance value X7R type capacitor (Fig. 4 had a significant decrease in capacitance with decreasing temperature. Design techniques must be employed to compensate for the change in value over the operating temperature range.

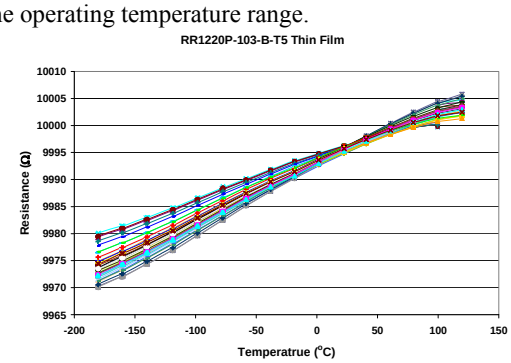


Fig. 1. Resistance as a function of temperature for Susumu Co., Ltd. high precision, RR series, 0.1%, 1/10 W thin film resistors (Data for 19 resistors)

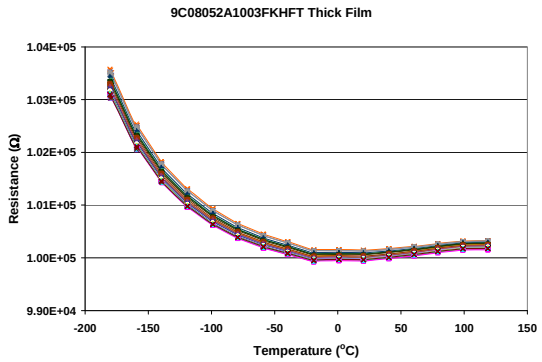


Fig. 2. Resistance as a function of temperature for Yageo America precision thick film chip resistors, 1%, 1/8 W. (Data for 19 resistors)

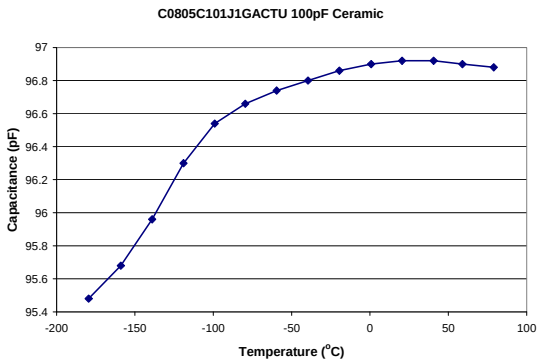


Fig. 3. Capacitance at 1MHz as a function of temperature for Kemet, NPO (COG) 100pF, 5%, 100V (Average of 5 capacitors)

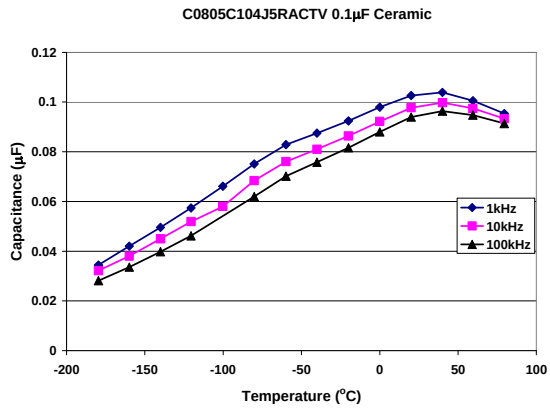


Fig. 4. Capacitance as a function of temperature for Kemet, X7R, 0.1µF, 5%, 50V (Average of 5 capacitors)

Fig. 5 shows the change in resistance for thick film resistors as a function of high temperature and resistor size, while Fig. 6 plots the change in resistance as a function of storage time at 500°C. With high temperature storage diffusion increases and interactions between the resistor material and the end terminations result in irreversible drift in the resistance value.

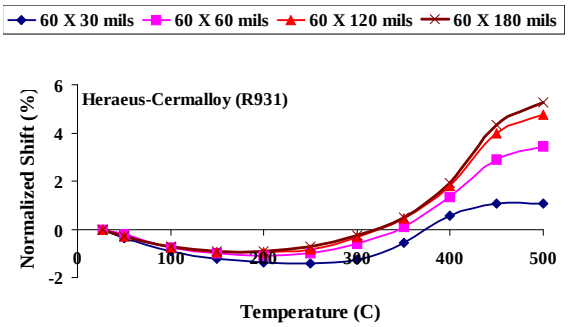


Fig. 5. Resistance as a function of temperature and resistor size for Heraeus 931 thick film resistors.

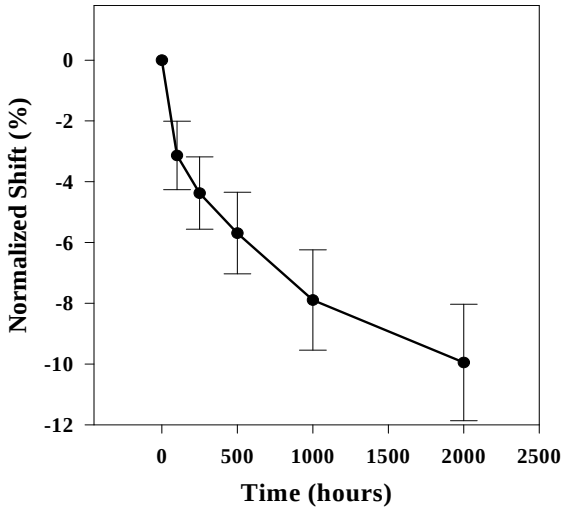


Fig. 6. Resistance as a function of storage time at 500°C for Heraeus 931 thick film resistors. Each data point is the average of 100 resistors and the error bars indicate 2 standard deviations about the average.

High temperature capacitors are a significant challenge. As shown in Fig. 7, the capacitance decreases significantly with increasing temperature. However, shown in Fig. 8, the capacitors are stable with aging at 300°C (Fig. 8). The high temperature storage test was performed without an applied bias voltage.

Active Devices – Under a contract from NASA ETDP under the RHESE program (M. Watson) a team lead by the Georgia Institute of Technology is developing silicon germanium (SiGe) device technology for low temperature applications. Addition of Ge to the base region of the bipolar transistor allows bandgap

engineering of the device. This can be used to optimize the device performance over the temperature range. SiGe BiCMOS technology is commercially available and combines Si CMOS devices with SiGe bipolar devices to fabricate integrated circuits.

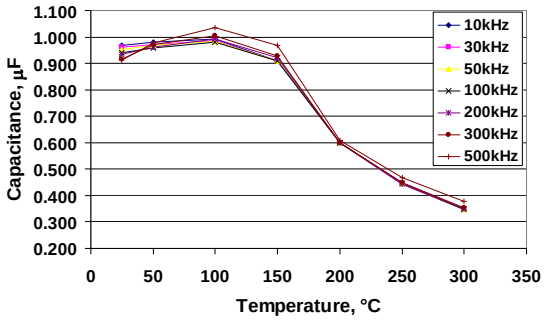


Fig. 7. Capacitance as a function of temperature for Calramic Technologies LLC ceramic capacitors.

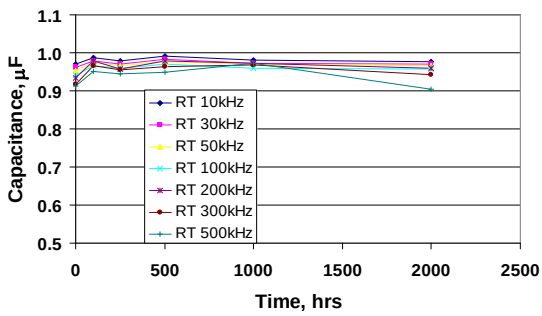


Fig. 8. Room temperature capacitance as a function of storage time at 300°C for Calramic Technologies LLC ceramic capacitors.

Fig. 9 shows the I-V characteristics of a SiGe heterogeneous bipolar transistor (HBT) at -230°C. The characteristics show good transistor action. Fig. 10 shows the output voltage of a bandgap reference as a function of temperature and bias voltage [1-4].

For high temperature applications, silicon-on-insulator (SOI) is being used for temperatures in the 200°C to 300°C range [5-6]. With traditional p-n junction isolation between transistors, the device leakage current increases with increasing temperature. Using SiO_2 to isolate transistors decreases the leakage current to acceptable levels at high temperatures. Increasing the doping levels of the p and n regions allows higher temperature operation before the junctions become intrinsic due to the relatively low bandgap (1.12eV) of silicon. Primary reliability concerns for high temperature operation of SOI are electromigration of the interconnect metallization and time-dependent breakdown of the gate dielectrics.

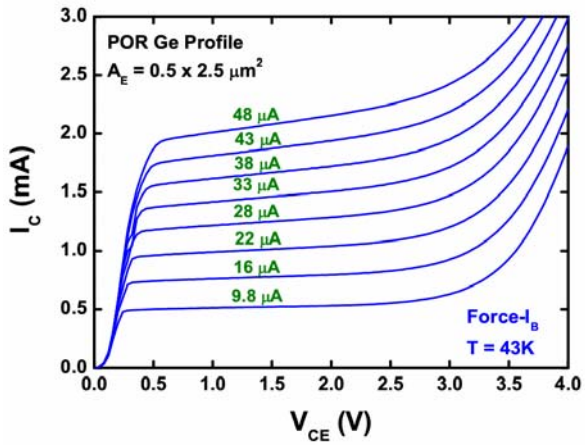


Fig. 9. SiGe HBT I-V characteristics at -230°C.

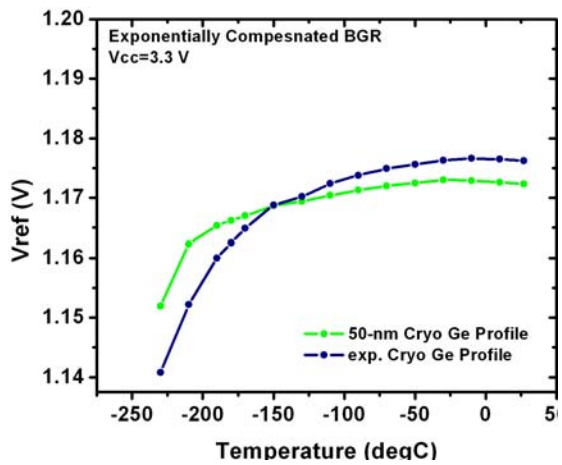


Fig. 10 SiGe Bandgap reference.

For higher temperature operation, wide bandgap devices such as silicon carbide (4H polytype-SiC: 3.26eV and 6H polytype-SiC: 3.03eV) and gallium nitride (Wurtzite polytype-GaN: 3.44eV) are being developed [7-10]. SiC transistors have been demonstrated to operate at 600°C. Fig. 11 shows the forward characteristics of 3 SiC static induction diodes in packaged in parallel for increase current capacity as a function of test temperature. Even at 400°C, the leakage current at low forward voltage is in the 10^{-8} to 10^{-7} amp range. For high temperature use, SiC devices are primarily being developed for power, communications and MEMS sensor applications, while GaN devices are being developed for communications and analog and digital integrated circuits.

Given the development and characterization of devices to support operation of electronics at extreme temperatures, interconnection and packaging becomes a critical element in building electronic systems

capable of operating in the extreme ambient environments.

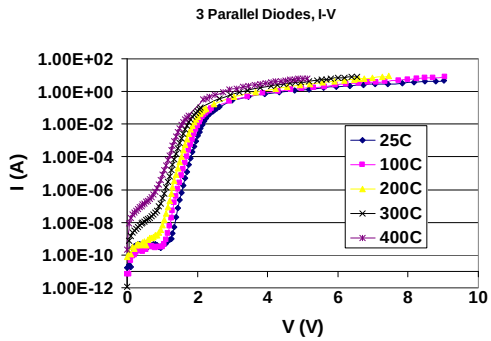


Fig. 11. Forward I-V characteristics of SiC static induction diodes as a function of temperature.

PACKAGING TECHNLOGY

Packaging provides the electrical interconnection between different devices and between the devices and the outside world. It also provides mechanical and environmental protection for the devices. A wide range of materials and processes are used to commercially package electronic devices. For low temperature package, changes in the mechanical properties of the packaging materials are a concern. For example, silicone encapsulant materials which are flexible and compliant at room temperature become rigid at -180°C. Low modulus silicone can act as a stress buffer between two materials with different coefficients of thermal expansion (CTE) in conventional temperature ranges. However, at low temperature the silicone has a much higher modulus, resulting in significant stress levels within the package.

At low temperatures, atomic movement and reaction rates are decreased. Therefore mechanisms, such as diffusion, grain growth, intermetallic formation and creep that affect the reliability of packages at room temperature and higher are not a concern. Thus, little degradation of packages left in the permanently shadowed craters of the moon would be expected.

For electronic packages on Mars or the surface of the moon subjected to periodic thermal cycling, the difference in the CTE of the devices and the packaging materials will have a large impact on reliability. With a lunar thermal cycle range of 300°C (-180°C to +120°C), even small differences in CTE will result in large stress levels between materials. Fatigue can occur in materials subjected to cycling stress, resulting in package failure. Also, with exposure to +120°C, diffusion, grain growth, creep and intermetallic formation can occur depending on the packaging materials. Diffusion can result in Kirkendall void formation due to differential diffusion rates between two metals. These voids coalesce to form cracks. Grain growth changes the mechanical properties of the material over time making it more susceptible to fatigue failure. Creep results in void formation leading to cracks an ultimately creep rupture of the material. Intermetallics are typically more brittle than the constituent elements. Formation of intermetallics can also consume thin metal layers leading to delamination at the interface.

At the high temperature extreme, the surface of Venus is a challenging environment. Most of the materials (epoxy, solder, silicone) used in conventional packaging melt or decompose at temperatures significantly below 485°C. Diffusion, grain growth, creep and intermetallic formation can occur rapidly at this temperature.

LOW TEMPERTURE PACKAGING

As part of the NASA ETDP project lead by Georgia Institute of Technology, Auburn University is leading the low temperature packaging effort. The packaging design philosophy is to develop multichip modules to reduce the levels of packaging required, i.e. rather than packaging each device individually and then interconnect between packages, interconnect the devices inside a common package. The material selection for the interconnect substrate and the package was driven by the need to minimize differences in CTE. The goal was to closely match the CTE of the SiGe (3ppm/^{o}C) die. Substrate options include Si, Si_3N_4 (3.2ppm/^{o}C) and AlN (4.5ppm/^{o}C). Initial package options considered were: Si_3N_4, AlN, Al_2O_3 (6.5ppm/^{o}C) and an aluminum-silicon alloy (7ppm/^{o}C). The ideal combination would be SiGe devices, Si or Si_3N_4 substrates and a Si_3N_4 package. Si_3N_4 substrates are available, but the commercial infrastructure does not exist for a Si_3N_4 package. Si_3N_4 package technology could be developed; however, without a commercial market the technology would not be cost effective for very low volume space applications. AlN packages are commercially available, but there are limited package varieties available as open tooling. Thus, while an AlN package could be used; there would be a substantial tooling charge for a custom package. From a CTE perspective, the Al_2O_3 and Al-Si alloy are very similar. Based on wide availability and cost, Al_2O_3 ceramic packages are currently being used.

Multilayer copper and polyimide layers are being deposited on Si, AlN and Si_3N_4 substrates to create the interconnections. Ti and Cu are deposited by e-beam evaporation to from a seed layer for pattern plating of Cu. The Cu layer is capped with a layer of Ni. Once the Cu and Ni are electroplated, the Ti/Cu seed layer is

etched away. The polyimide is applied by spin coating and then cured. HD Microsystems PI-2211 polyimide is used. PI-2611 has a CTE of 3ppm/°C in the x-y plane. An Al layer is e-beam evaporated and patterned to serve as an etch mask for reactive ion etching (RIE) of vias in the polyimide. After RIE, the Al is stripped. This process is repeated to fabricate a multilayer interconnection pattern. For assembly, the top metal layer is Ti/Cu/Ni/Au. This metal stack is compatible with Au thermosonic wire bonding and flip chip assembly. Fig. 13 shows an SEM micrograph of a three layer metal structure with vias.

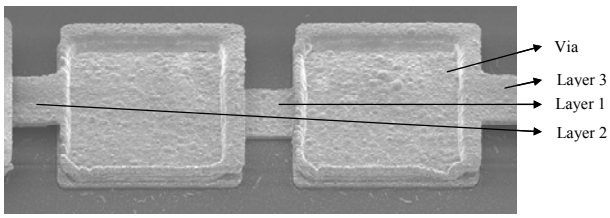


Fig. 12. SEM micrograph of a daisy chain test structure with three layers of metal and interconnecting vias.

For wire bond assemblies, an AlN substrate is being used in the package for interconnecting the SiGe die. This provides an intermediate CTE between the SiGe die and the Al_2O_3 package. Indium is being used for both substrate-to-package and SiGe die-to-substrate attachment. Indium remains malleable at -180°C, minimizing stress between the package and substrate and between the substrate and SiGe die. A proprietary backside metallization has been developed, compatible with In die attach. The In soldering is done in a vacuum furnace to minimize void formation in the die and substrate attach layers. Figure 13 plots the effect of aging at 125°C on die shear strength. After an initial decrease in shear strength the shear strength remained stable though 1000 hours. The results indicate no brittle intermetallic or void formation with aging.

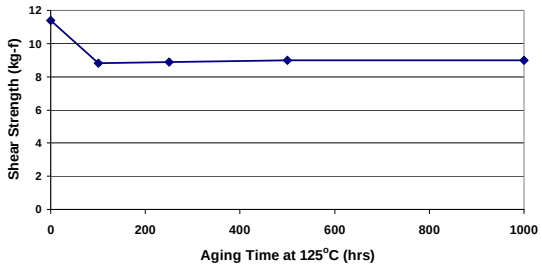


Figure 13. Die Shear Test Results for a 5 mm x 5 mm Si Test Die as a Function of Storage at 125°C.

As a first thermal cycle screening, 5mm x 5mm die attached to substrates (approximately 46mm x 13.5mm) in packages were subjected to 50 liquid thermal shock cycles. The package was a 40 pin Al_2O_3 ceramic dual-inline package with a cavity size of 49mm x 14.4mm. One liquid was liquid nitrogen (-196°C) and the other was heated fluorinert (+125°C). There were no failures of the die-to-substrate or substrate-to-package attachment. Nor was there any observable damage to the polyimide/metal interconnect structure. More detailed thermal cycling tests are planned to establish the reliability of the assembly materials and processes. Figure 14 show a photograph of a wire bonded test die.

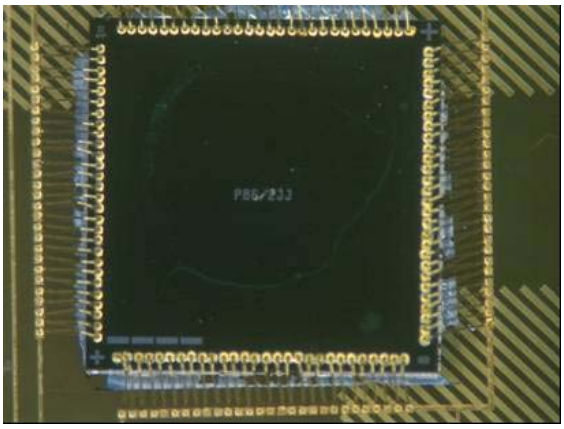
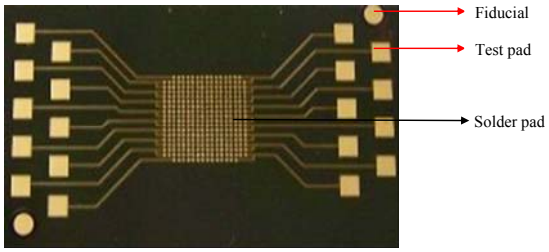
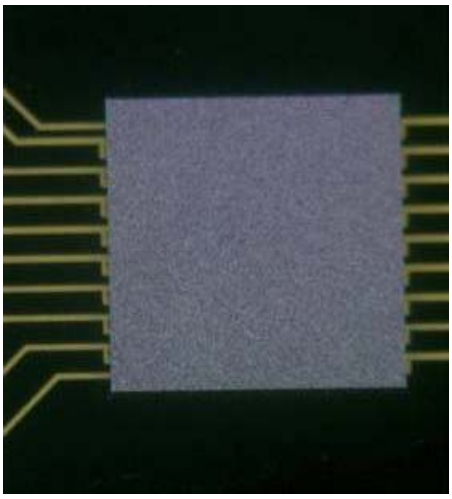


Fig. 14. Photograph of a wire bonded test die.

For flip chip assembly of the SiGe die, a Si or Si_3N_4 substrate is being used to match the CTE of the SiGe die. In conventional flip chip assembly, underfill is used to minimize the strain on the solder joints due to the CTE mismatch between the die and the substrate. However, the CTE of the underfill ranges from 25-45ppm/°C depending on the manufacturer and formulation. With a 300°C temperature range, this high CTE will place a large tensile stress on the underfill at -180°C. With a matched die and substrate CTE and the use of a malleable In/Pb (50/50) solder bump, no underfill was used in the initial assembly. An example of the flip chip substrate and assembly are shown in Fig. 15.



a. Flip chip substrate pattern



b. Assembled flip chip

Fig. 15. Example of flip chip assembly.

As a first evaluation, two sealed flip chip packages were subjected to 50 liquid thermal shock cycles. The substrate was approximately 46mm x 13.5mm. The package was sealed by soldering with eutectic Sn/Pb solder in a vacuum furnace. One liquid was liquid nitrogen (-196°C) and the other was heated fluorinert (125°C). The parts were held at each temperature to allow them to reach equilibrium and rapidly transitioned (manual) between the two liquids. The flip chip solder joints did not fail after 50 cycles. There was no failure of the Si substrate-to-Al_2O_3 package indium attachment or of the Sn/Pb package solder seal. Additional tests are planned to establish the reliability of the material set and module construction.

Two versions of a two SiGe die wire bonded module have been fabricated to demonstrate the technology. The first, shown in Fig 16 is a small cavity 40 pin dual-inline package. The second package (Fig. 17) is the larger cavity 40 pin dual-inline package used for the wire bond and flip chip assembly experiments. The larger cavity package allowed the inclusion of discrete passive components. Work is now underway to develop process compatible thin film resistors and capacitors that will be fabricated as part of the multilayer Cu/polyimide substrate.

HIGH TEMPERATURE PACKAGING

SOI devices can be used at temperatures up to 300°C. A multichip packaging approach based on thick film hybrid technology has been investigated [11]. For evaluation of the assembly processes and materials, silicon test die (5mm x 5mm) with a thin film backside metallization (80nm Cr/200nm Pt/300nm Au) were fabricated. Eutectic Au-Ge preforms were selected for die attach. With a melting point of 356°C, Au-Ge should be suitable for use to 300°C. The Au-Ge will not form intermetallics with the thick film metallization or the die backside metallization. Au-Ge performs 1.0 mil thick were used to attach the die to DuPont 5771 thick film gold metallized Al_2O_3 substrate. A vacuum solder system was used for the die attach. Samples were fabricated with little or no voiding as determined by x-ray inspection. Fig. 18 shows the shear strength as a function of storage time at 300°C. After an initial increase in shear strength, the shear strength remained relatively constant (within the normal scatter of die shear measurements) through 2000 hours at 300°C indicating no degradation mechanism.

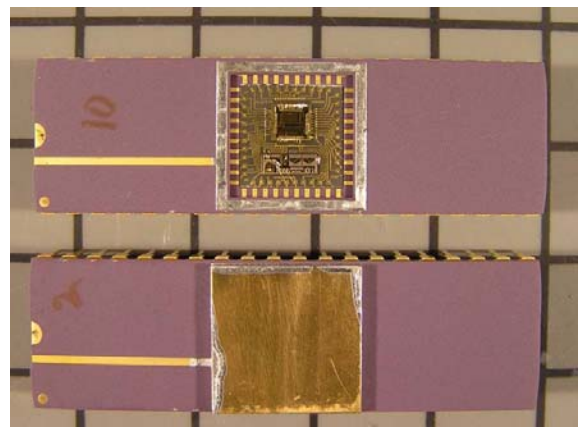


Fig. 16. Photograph of small cavity 40 pin package.

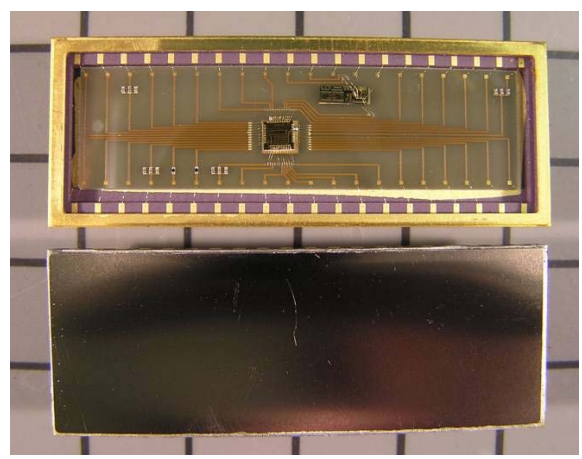


Fig. 17. Photograph of large cavity 40 pin package.

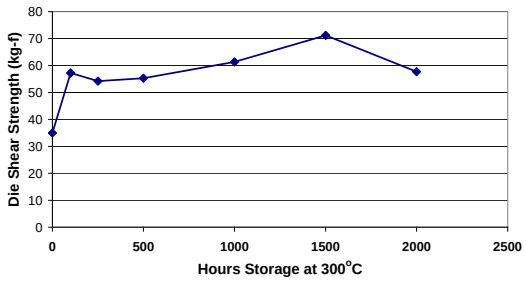


Fig. 18. Die shear strength as a function of aging at 300°C.

If thermal cycling is required, the CTE mismatch between the Al_2O_3 and the SOI die will be a major reliability concern. Fig. 19 shows an example of cracking of both the AuGe die attach material and the Si die after 500 thermal cycles between +40°C and +300°C. The die was 5mm x 5mm attached to an Al_2O_3 substrate metallized with DuPont 5771 thick film Au. Additional work is required in this area. Metallization techniques are being developed for AlN and Si_3N_4 substrates.

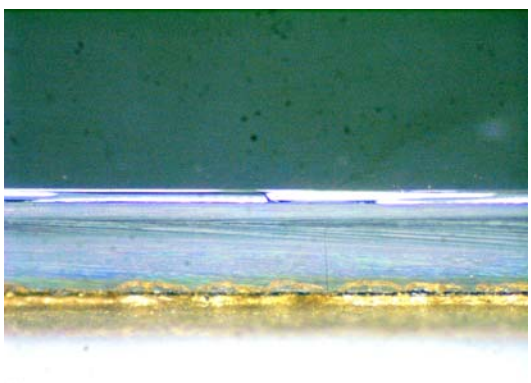


Fig. 19. Example of die attach and Si cracking after 500 thermal cycles from +40°C and +300°C on a thick film Al_2O_3 substrate.

SOI devices typically have Al wire bond pads. At temperatures above 200°C, Au-Al intermetallic formation and Kirkendall voiding would limit reliability. Electroless Ni/electroless Au plating was used to cap the Al layer. This is a maskless process compatible with post wafer processing. Electroless Ni/Immersion Au is commonly used as an under bump metallization for flip chip die. For Au and Pt thermosonic wire bonding, a thicker Au layer (1-1.5μm) is needed and was deposited by electroless plating. DuPont 5771 Au ink was printed on Al_2O_3 substrates for this test. The Au wire was 1.0 mil diameter, 2-6% elongation, and a minimum tensile strength of 9 grams.

Figs. 20, 21, and 22 plot the Au ball shear strength, the wire pull strength and the daisy chain resistance around a die as a function of storage time at 300°C. Each data point in the pull and shear strength data represents the average of 50 measurements. Each resistance data point through 1000 hours of storage represents the average of 28 daisy chain resistance measurements. To extent the test beyond the originally planned 1000 hours, wire bonds from resistance test die were used for pull and shear testing. At the 10,000 hour measurement, the resistance data point represents the average of 11 resistance measurements.

The ball shear measurement shows an initial increase in shear strength, and then remains relatively stable. The daisy chain resistance shows a slight initial decrease in resistance and then remains relatively stable. The Ni barrier layer (nominally 3μm thick) was effective in preventing Au-Al diffusion through 10,000 hours at 300°C. The decrease in wire bond pull strength with time is a result of annealing of the Au wire. No bond lifts were observed. However, there is significant increase in the elongation of the wire prior to failure during pull testing with aging at 300°C.

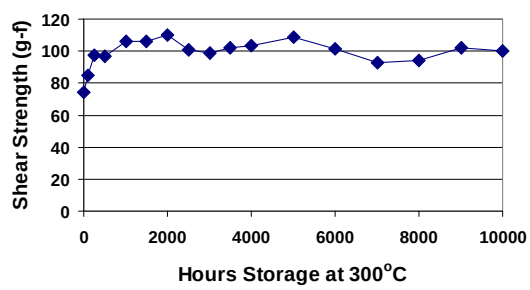


Fig. 20. Gold ball shear strength as a function of storage time at 300°

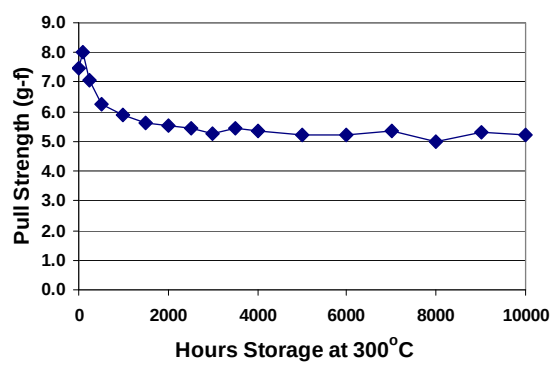


Fig. 21. Gold wire pull strength as a function of storage time at 300°C.

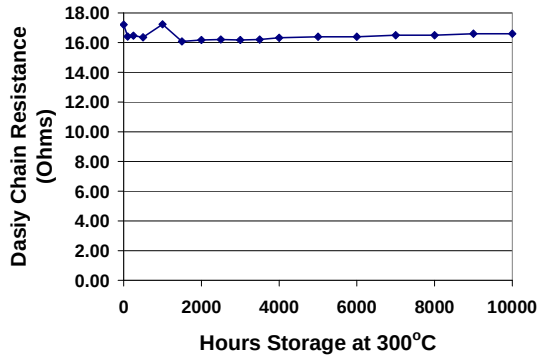


Fig. 22. Gold wire bond daisy chain resistance as a function of storage time at 300°C.

SiC die attach has also been investigated [12]. The die attach material must be compatible with the substrate and die backside metallization, have a sufficiently high melting point after die attach and not form intermetallics which degrade the bond strength with time at temperature. The die attach material used in this research was off-eutectic AuSn. The primary compatibility concern was the reactivity of the Sn with the die backside metallization. A sputtered three layer thin film stack composed of Ti/Ti-W/Au (1000 Å /2000 Å /2000 Å) was evaluated as the chip metallization. Ti provides good adhesion to the device contacts (Ni_2Si, an ohmic contact); Ti-90W functions as a diffusion barrier layer; and Au protects the underlying Ti-W from oxidation, as well as provides a wire bondable and braze wettable surface. Sn does not form intermetallics with W, but does with Au, Ti and Ni. Ni may remain as residual Ni after the formation of the Ni_2Si on the SiC die.

The die attach technique developed uses a eutectic Au-Sn preform (3.3 mm x 3.3 mm x 0.020 mm) with thick Au (20 µm) plating either on the substrate or on the chip. With high temperature brazing and annealing at 400°C, the Sn from the eutectic Au-Sn preform diffuses into the thick Au layer, lowering the Sn concentration to less than 10 wt% and raising the alloy melting point to over 400°C.

The brazing process was performed with an vacuum furnace. Voids in the bonding layer will significantly hinder the heat transfer from the chip to the substrate and weaken the braze joint strength. In order to obtain a void-free bond, the process was run in vacuum, and a 20 g weight was placed on the assembly to create some flow of the AuSn when it melts. The chip size was 3.75 mm x 3.75 mm with Ti/Ti-W/Au (20µm) metallization, and the direct bond copper (DBC) Al_2O_3 substrate size was 5 mm x 5 mm. DBC substrates are commonly used in power modules: the thick Cu layer provides high current carrying capability.

A void-free die attach was achieved and verified by x-ray. The bond strength was evaluated by a die shear test utilizing the Dage PC2400 system. The average as-brazed sample die shear strength was > 100kg-f (equipment limit). The sample size was seven.

A high temperature storage test (400°C) was used to determine the effect of time and temperature on the die shear strength. In order to study the effect of Ni as a diffusion barrier and reaction layer, two types of DBC Al_2O_3 substrate were used in this test: DBC Al_2O_3 with electroless plated Ni:P and DBC Al_2O_3 with electrolytic plated Ni. The Ni layers were approximately 6 µm thick, protected by a 0.10-0.20 µm layer of immersion Au. To lower the Sn concentration to less than 10 wt%, a thick Au (20 µm) layer was required, and two sources of thick Au metallization were used in this study: thick Au plated on the chip backside and thick Au plated on the substrate. It is easier to electroplate the wafer (dicing the wafer into individual chips afterward) than to electroplate the individual DBC Al_2O_3 substrates, which is time consuming. On the other hand, with the immersion gold surface finish, Ni and Cu will diffuse through the immersion gold to the top of the substrate surface and oxidize in air during high temperature storage. A thick Au layer (20 µm) on the substrate will help to retard the diffusion and subsequent oxidation of the underlying Ni and Cu layers. In summary, four kinds of samples were built for the high temperature storage test:

- DBC on Al_2O_3 with electroless Ni:P, thick Au on substrate
- DBC on Al_2O_3 with electroless Ni:P, thick Au on chip
- DBC on Al_2O_3 with electrolytic Ni, thick Au on substrate
- DBC on Al_2O_3 with electrolytic Ni, thick Au on chip

The samples were tested at 100 hours, 250 hours, 500 hours, 1000 hours and 2000 hours with a group sample size of seven. A die shear test was used to evaluate the braze joint strength, and a cross-section sample was subjected to scanning electron microscopy /energy dispersive x-ray (SEM/EDX) analysis in order to detect intermetallic compound (IMC) formation and elemental interdiffusion during high temperature storage.

Figure 23 shows the die shear values for the four types of samples after aging at 400ºC. The Dage PC 2400 used to perform this test has a 100 kg-f shear strength limit. The die shear strength of the electrolytic Ni samples (both thick Au on substrate and on chip) did not degrade after 2000 hours of thermal storage. However, the average die shear strength of the

electroless Ni:P samples with Au on the substrate and Au on the chip degraded to 77.2 kg and 73.6 kg, respectively after 2000 hours aging at 400ºC in air.

Fig. 24 presents an EDX element composition cross-section analysis of the braze interface after 2000 hours storage at 400ºC. The metallization of the DBC Al_2O_3 substrate was Cu/ Ni:P/ immersion Au, with a thick Au (20µm) layer on the chip. The following conclusions can be drawn:

1. A semi-continuous Ni:P:Cu layer formed during aging.
2. The AuSn braze layer was almost depleted of Sn, with only a residual level (about 1 wt%) of Sn remaining in the layer. Sn continued to react with Ni and Au, forming intermetallic compounds during aging. The Ni-Sn-Au intermetallic compounds were separated from the Ni:P:Cu under layer by a layer of 85 wt% Au-15 wt% Cu.
3. Cu was able to diffuse through the Ni:P and was found everywhere in the Au layer. Au was only able to diffuse into the Cu layer at the location where the Ni:P:Cu layer was physically broken.

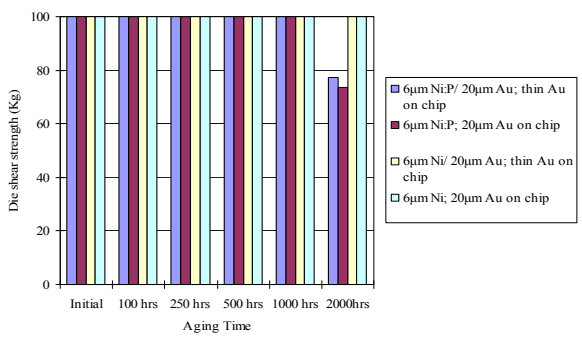
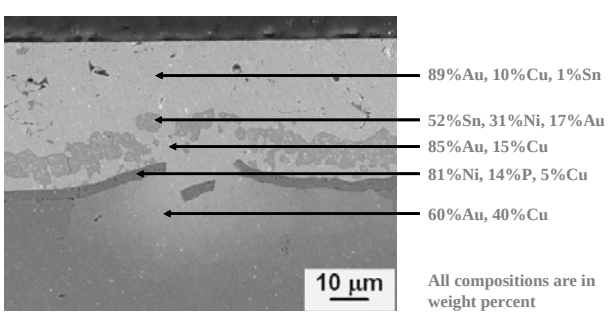
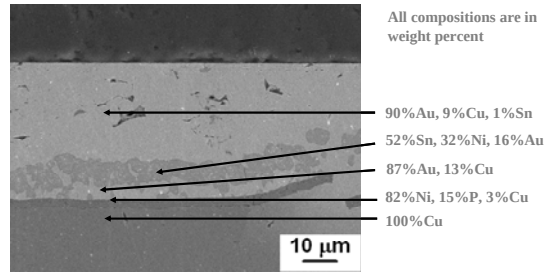


Fig. 23. Die shear strength as a function of aging at 400ºC in air.



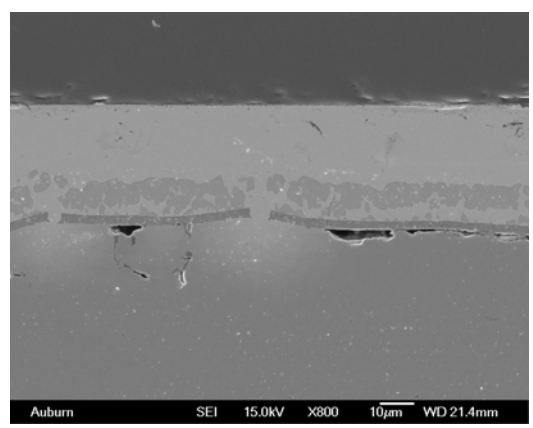
(a)



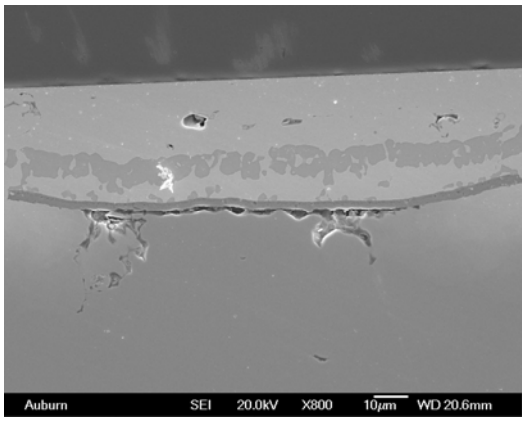
(b)

Fig. 24. Cross-section of die attach after 2000 hours at 400ºC, electroless Ni:P, thick Au on chip, (a) at Ni:P:Cu broken area and (b) at Ni:P:Cu continuous area

Fig. 25(a) shows voids that developed at the Cu-Ni:P interface after 1000 hours aging at 400ºC, and Fig. 25(b) shows a crack that developed at the Cu-Ni:P interface after 2000 hours aging at 400ºC. Kirkendall voiding is the formation of voids due to different interdiffusion rates between two neighboring materials. Cu and Au are completely miscible. During high temperature aging, Cu diffuses into the Ni and Au layers, but at the same time there is negligible diffusion of Ni and Au in the opposite direction into the Cu across the Cu-Ni:P interface (Fig. 24(b)). The Ni:P layer is an effective barrier to Au diffusion (except in Fig. 24(a) where the layer is physically broken. The net result is that atomic vacancies are generated in the Cu. As the diffusion proceeds, the vacancy concentration increases until super-saturation occurs, resulting in nucleation and the growth of voids (Kirkendall voids). The different interdiffusion rates across the Ni:P layer caused voids to occur at the Cu-Ni:P interface after 1000 hours aging at 400ºC (Fig. 25(a)) and the coalescence of these voids resulted in cracks at the Cu-Ni:P interface after 2000 hours of thermal storage (Fig. 25(b)). The lower die shear strength was due to occurrence of these cracks.



(a)



(b)

Figure 25. Cross-section of the die attach, (a) voids at Cu-Ni:P interface after 1000 hours aging and (b) cracks at Cu-Ni:P interface after 2000 hours aging at 400ºC.

Fig. 26 presents an EDX element composition cross-section analysis of the braze interface after 2000 hours storage at 400ºC for the electrolytic Ni, thick Au on the substrate sample. These results lead to the following observations:

1. A series of intermetallic compounds was formed, consuming the Sn and the Ni layer.
2. Cu was able to diffuse through the Ni into the Au layer.
3. The complex intermetallics formed had good adhesion and strength after aging.

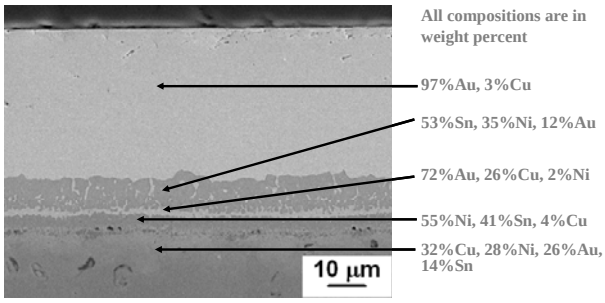


Fig. 26. Cross-section of die attach after 2000 hours at 400ºC, electrolytic Ni, thick Au on substrate

Fig. 27 shows small voids that developed at the Cu-Ni interface after 2000 hours aging at 400ºC. Kirkendall voiding can explain the void formation at the Cu-Ni interface due to the differential diffusion rates. However, because Au, Ni and Sn diffused into the Cu layer, the voids that developed at the Cu:Ni interface were smaller and less frequent than those that developed at the Cu-Ni:P interface, and no crack developed at the Cu-Ni interface which is consistent with the die shear strength (>100kg-f) after 2000 hours aging. The Ni layer was a less effective barrier than the Ni:P to Au and Sn diffusion into the Cu layer.

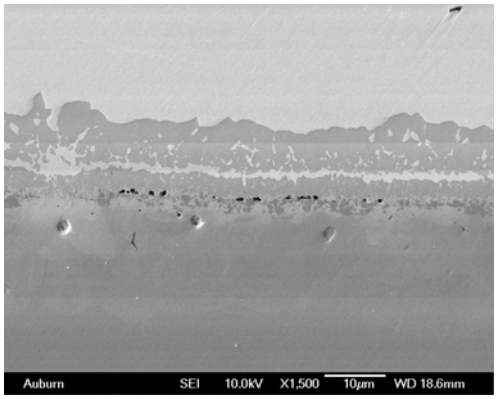


Fig. 27. Cross-section of the die attach, showing voids at Cu-Ni interface after 2000 hours aging at 400ºC

Additional work is required to develop die attach materials and process for applications above 400°C. Furthermore, only limited thermal cycling experiments have been performed, but initial results indicate that significant work must be done if the application requires thermal cycling over wide temperature ranges. This is particularly true for power module substrates with thick Cu. Fig. 28 is an cross section micrograph of a SiC die attached to a DBC Al_2O_3 substrate after 300 thermal cycles between +35°C and +400°C. There is cracking of both the die attach material and the ceramic substrate underneath the Cu foil.

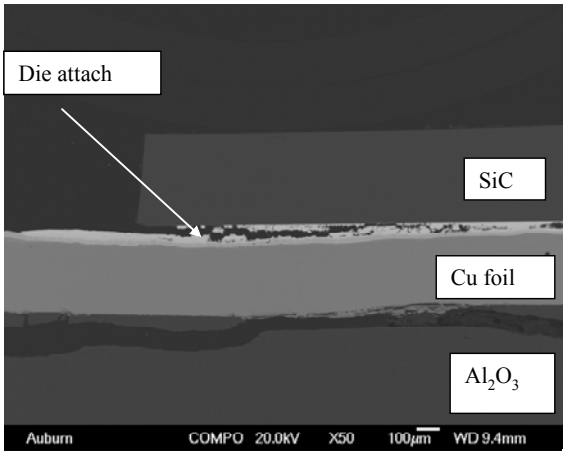


Fig. 28. Micrograph of a SiC die attached to a DBC Al_2O_3 substrate after 300 thermal cycles between +35°C and +400°C.

SiC die typically have Au wire bond pads. Thus, with Au thermosonic wire bonding there is no concern as this creates a monometallic system with the die bond pad and the Au substrate metallization. Figs. 29 and 30

show wire bond test results for 250µm diameter Au wire bonded to Cu/Ni/Au metallized ceramic substrates and to Ti/Ti:W/Au metallized SiC test die. While the shear strength decreases due to annealing of the Au wire, there is no catastrophic decrease in strength.

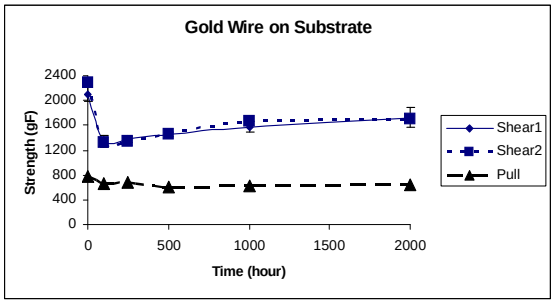


Fig. 29. Average pull/shear strength of platinum wire on Cu/Ni/Au substrate metallization as a function of storage time at 300°C.

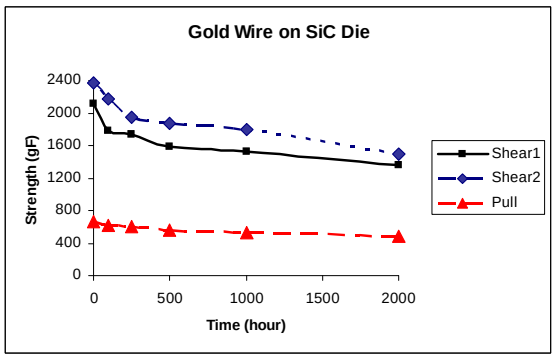


Fig. 30. Average pull/shear strength of Au wire on Ti/Ti:W/Au die metallization as a function of storage time at 300°C.

SUMMARY

There are a number of advantages to distributed electronic systems capable of operating in the extreme ambient environments encountered by space probes. Device and packaging technologies are currently under development which can make this possible. Challenges still remain, but significant progress has been made in understanding the issues and selecting the materials and assembly processes necessary.

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